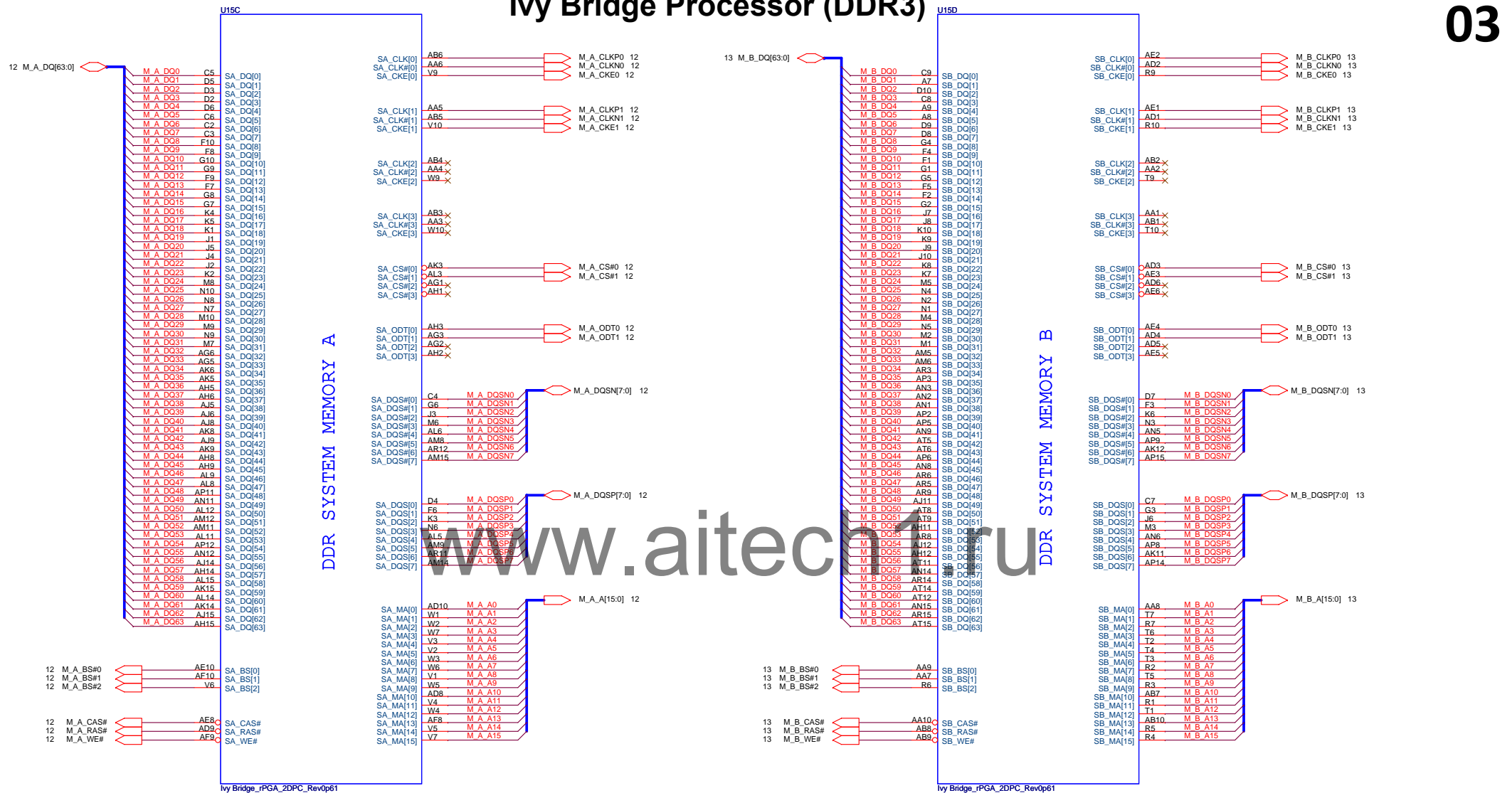


## Ivy Bridge Processor (DDR3)



Ivy Bridge\_rPGA\_2DPC\_Rev0p61

Ivy Bridge\_rPGA\_2DPC\_Rev0p61

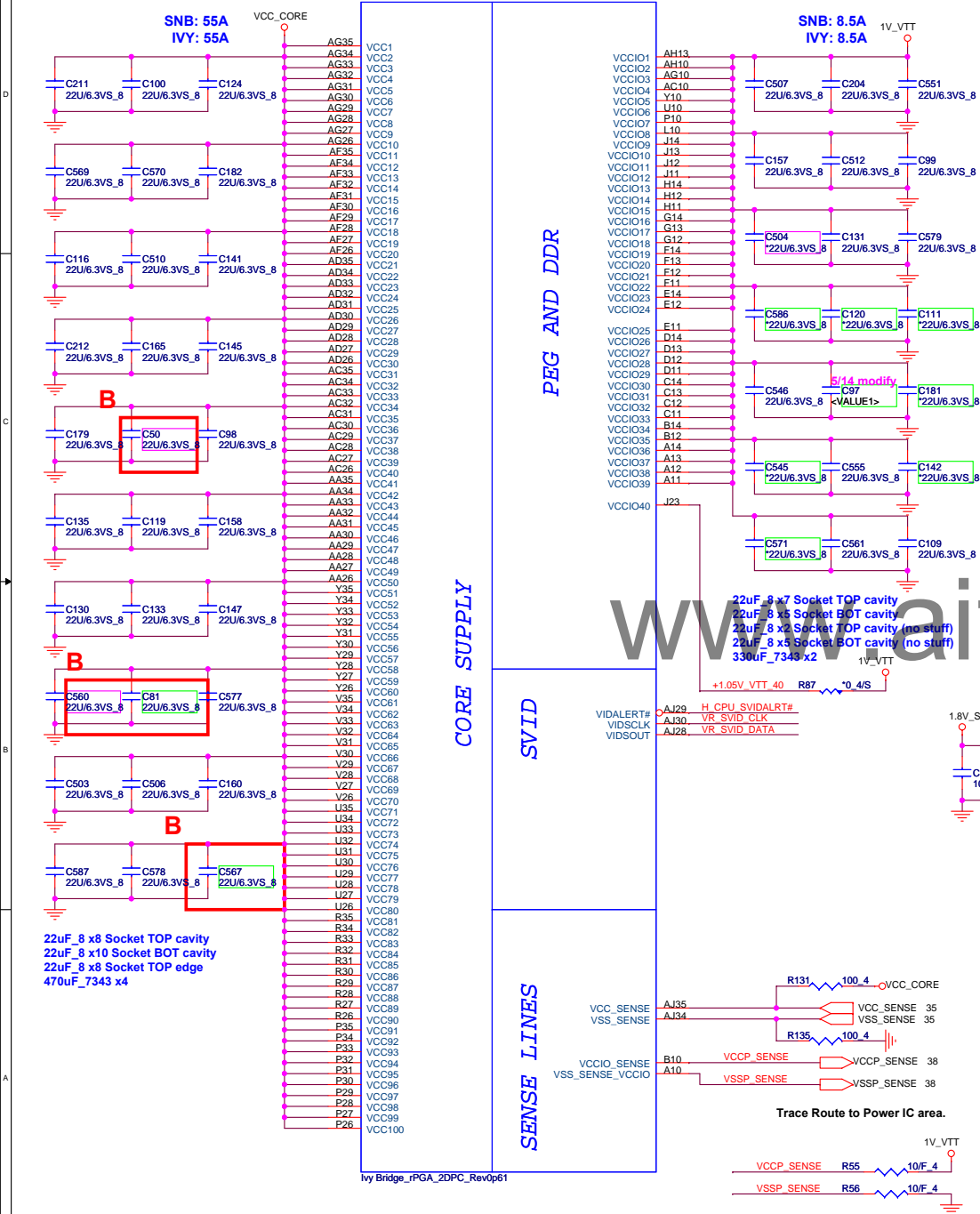


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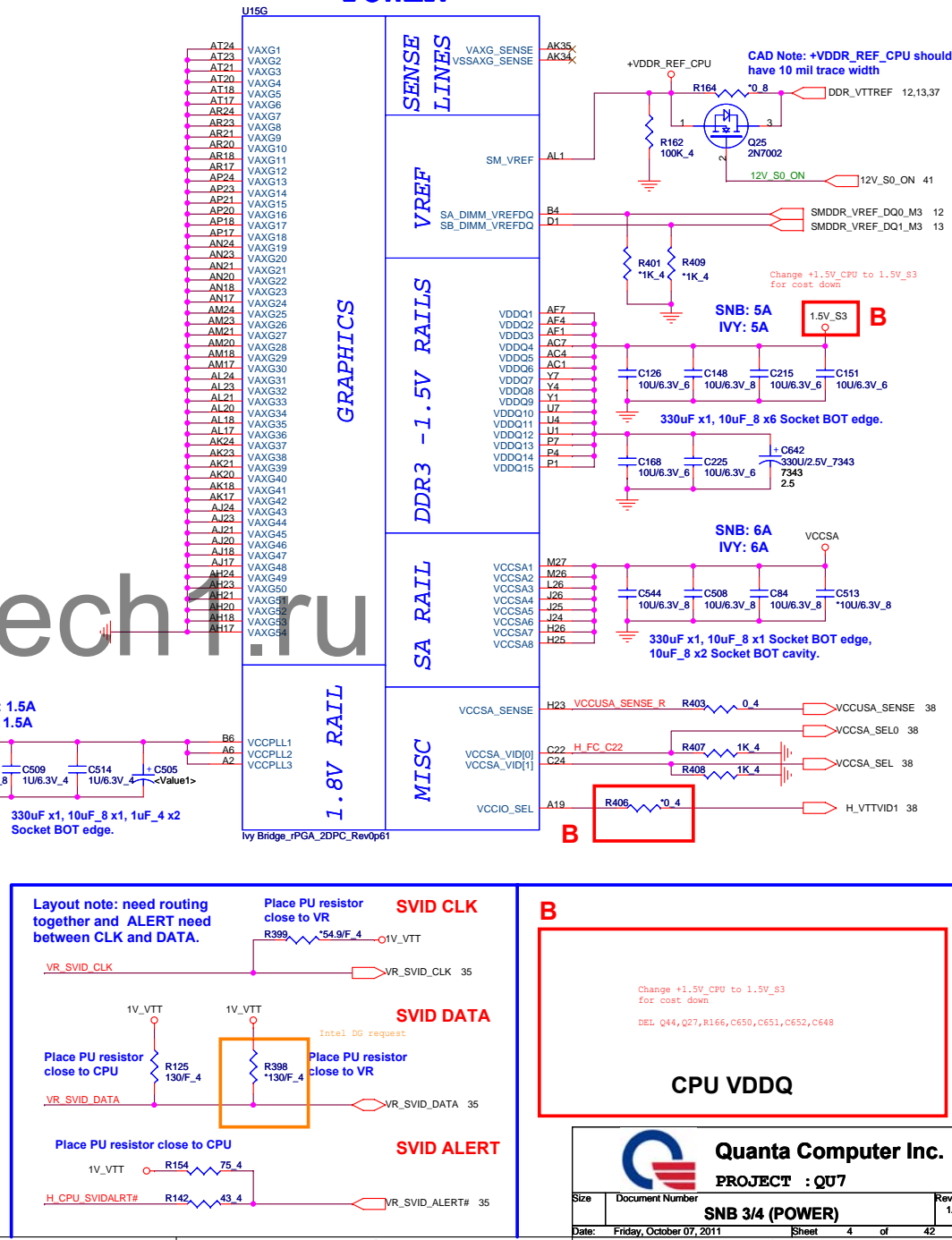
PROJECT : QU7

Size	Document Number	Rev
	<b>SNB 2/4 (DDR3 I/F)</b>	1A
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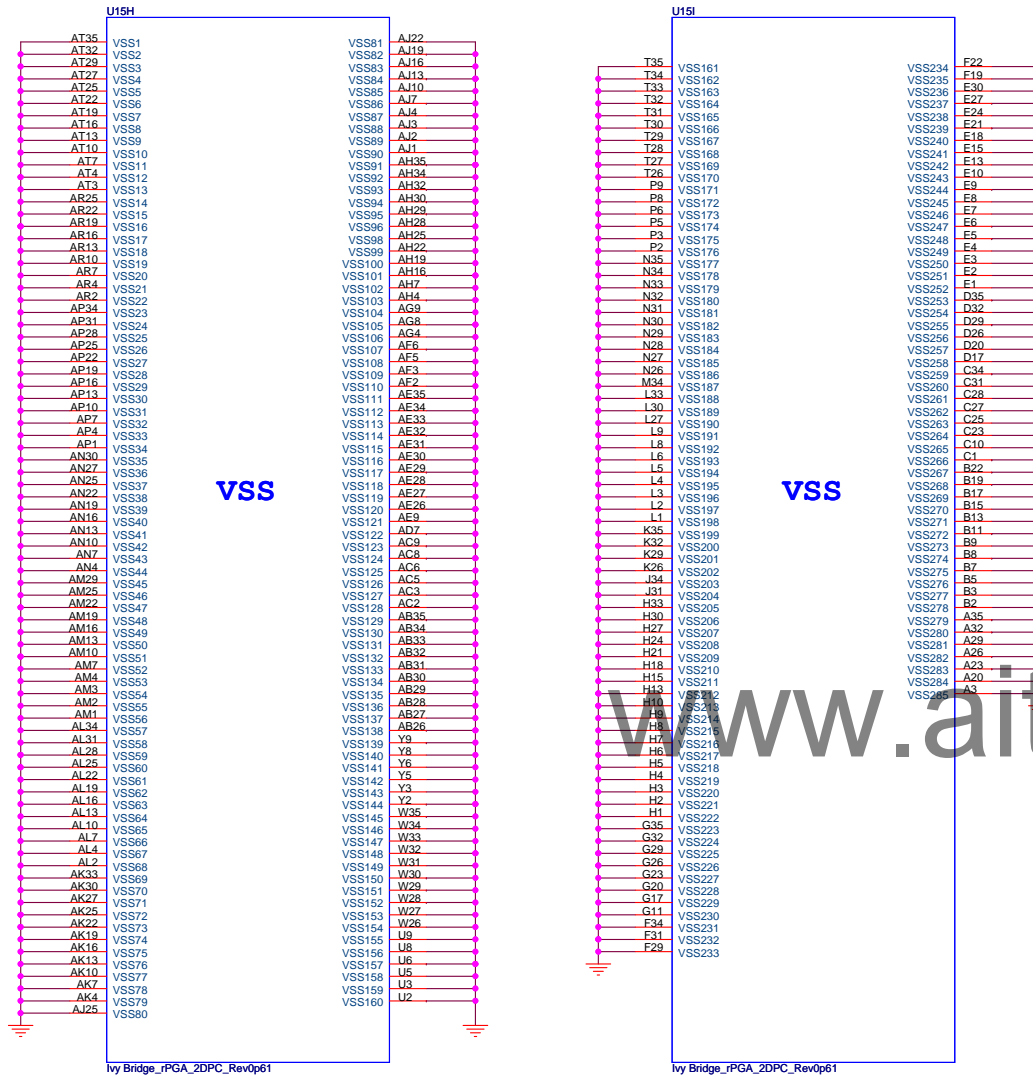
## POWER



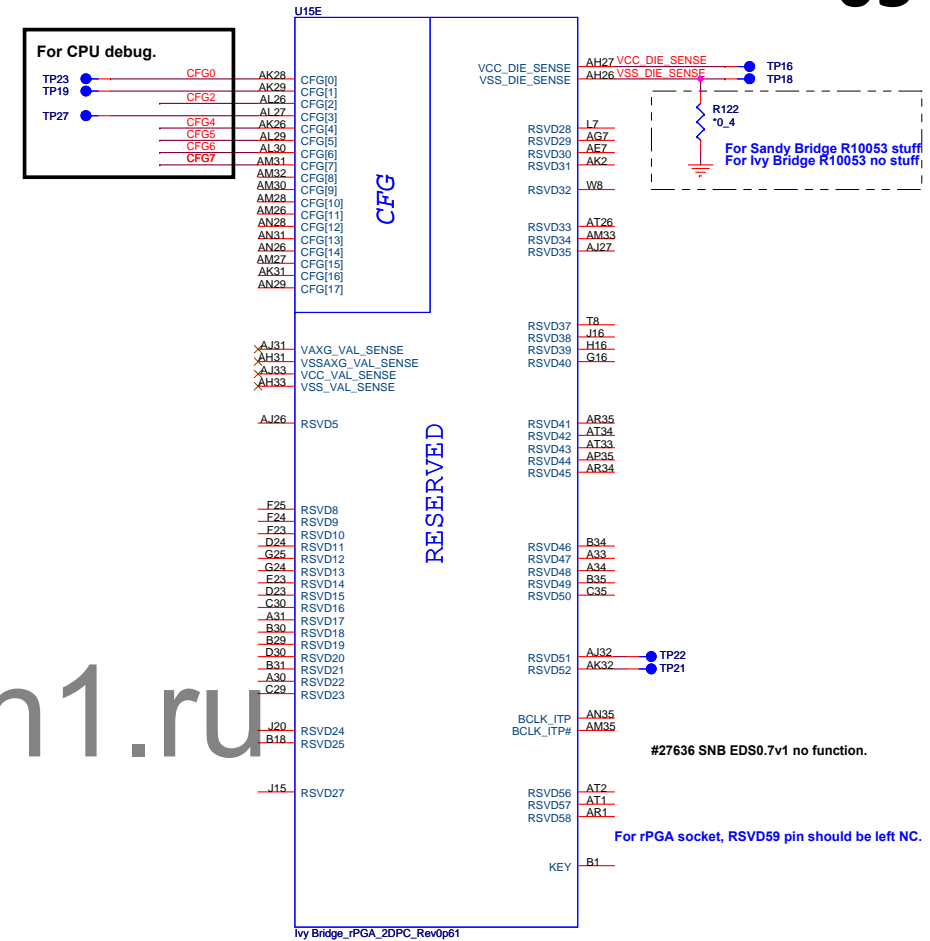
## POWER



## Ivy Bridge Processor (GND)



## Ivy Bridge Processor (RESERVED, CFG)

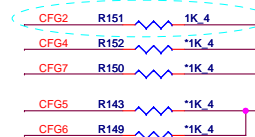


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

(hh) TWH PEG bus is Lane Reversed



## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

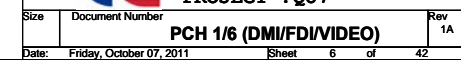


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PROJECT : QU7

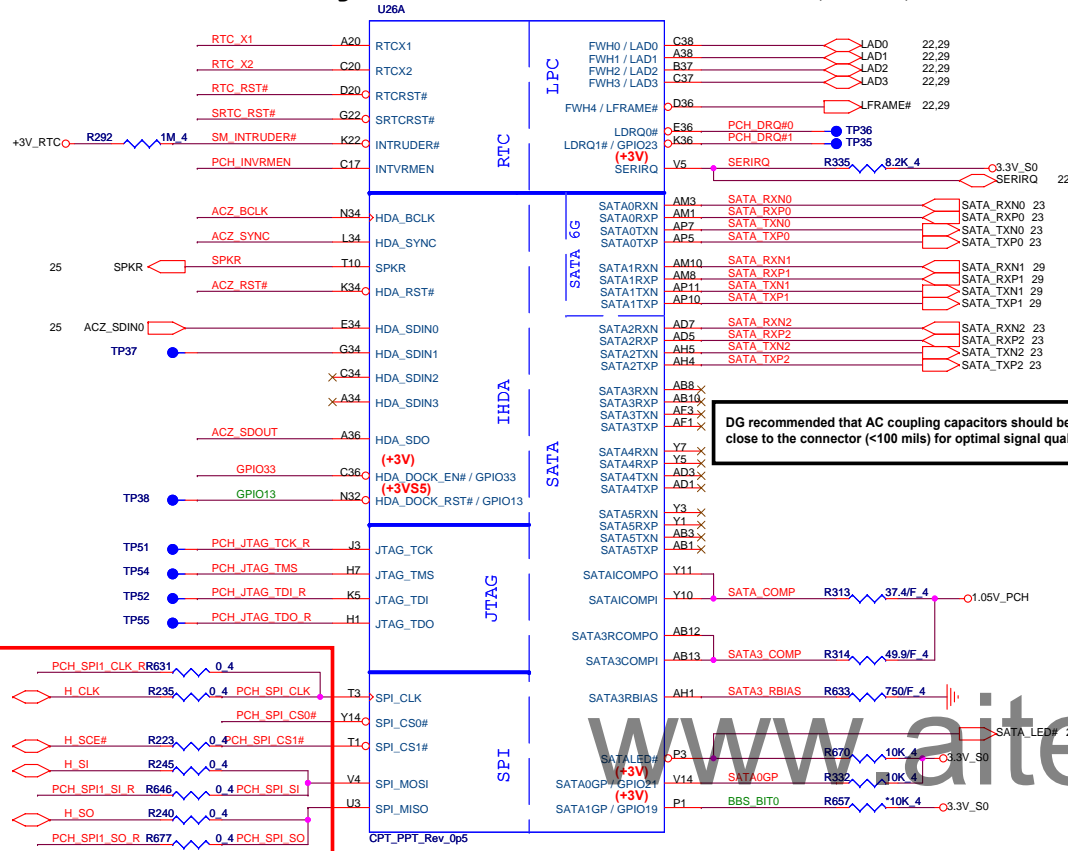
Size	Document Number	Rev
	<b>SNB 4/4 (GND)</b>	1A
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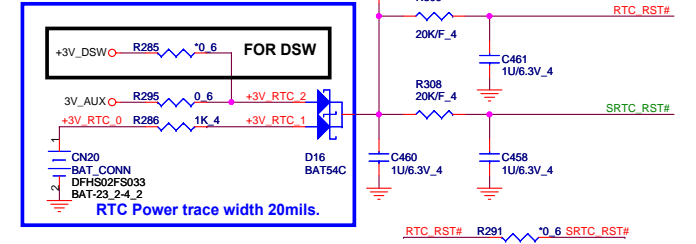


# Cougar Point/Panther Point (HDA,JTAG,SATA)

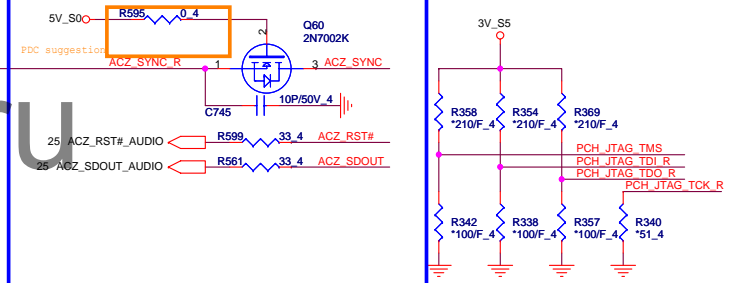
07



## RTC Circuitry(RTC)



## HDA Bus(CLG)

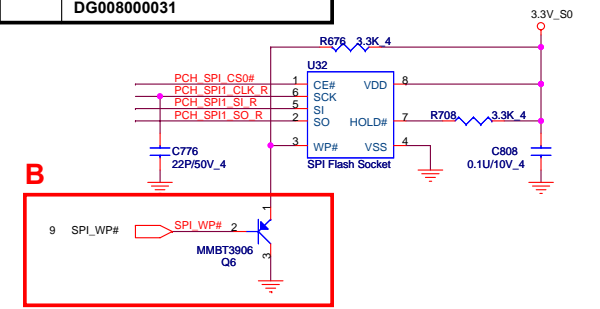


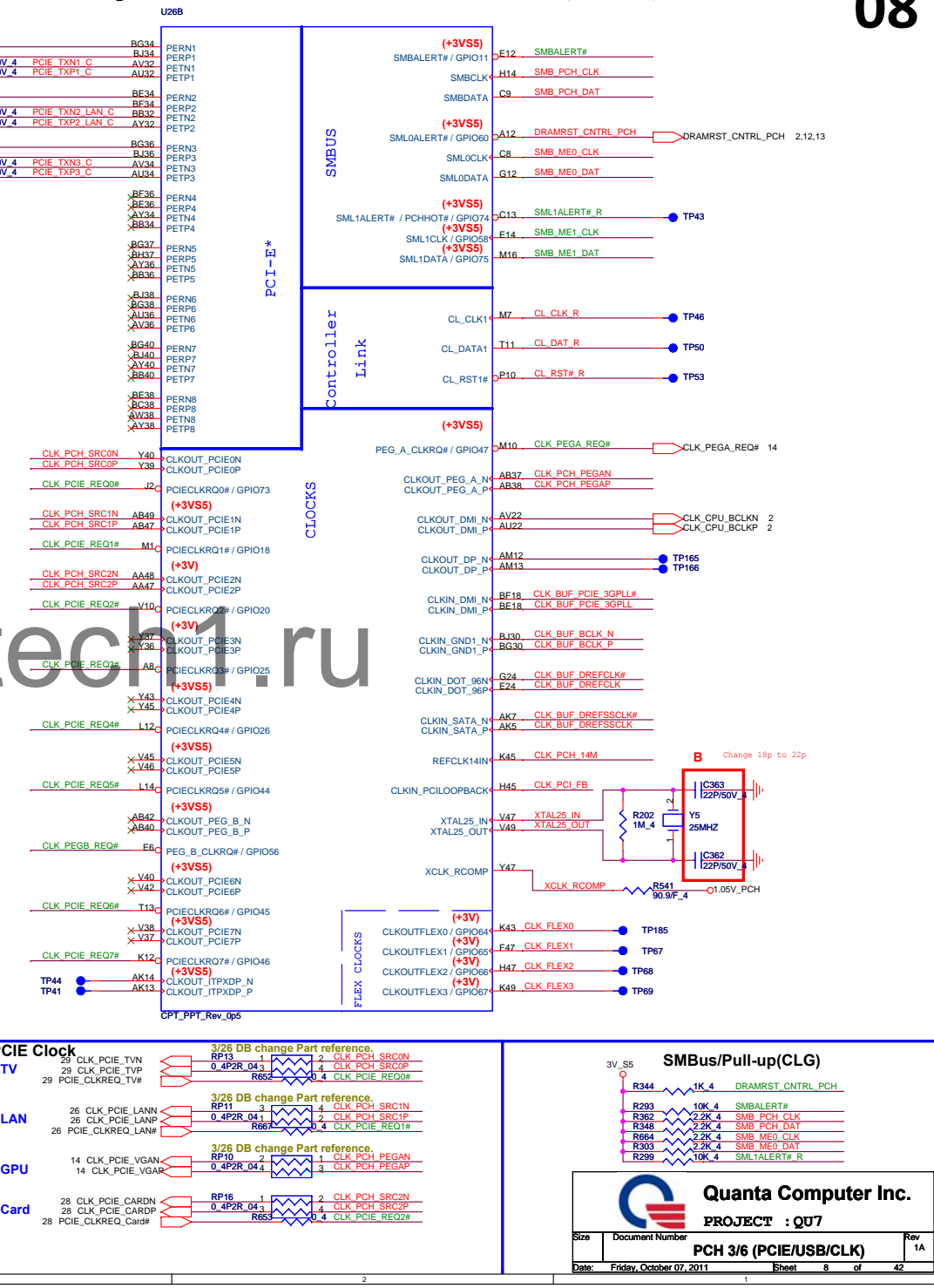
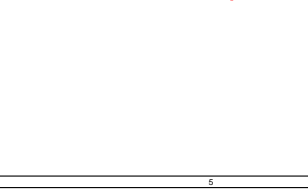
## PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R666 1K_4 3.3V_S0
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	3.3V_S0 R548 1K_4 R546 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R593 330K_4 3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R566 1K_4 GPIO33_E GPIO33_E 22
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	BBS_BIT0 R630 1K_4 BBS_BIT1 R647 1K_4
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	1.8V_SFR R635 1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	1.8V_SFR R644 2.2K_4 R634 1K_4 NV_CLE 9 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S0 R594 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R571 1K_4 V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R639 1K_4 ICC_EN 9
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R648 1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R622 1K_4 3.3V_S0

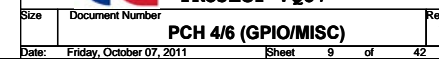
Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

## PCH SPI ROM(CLG)

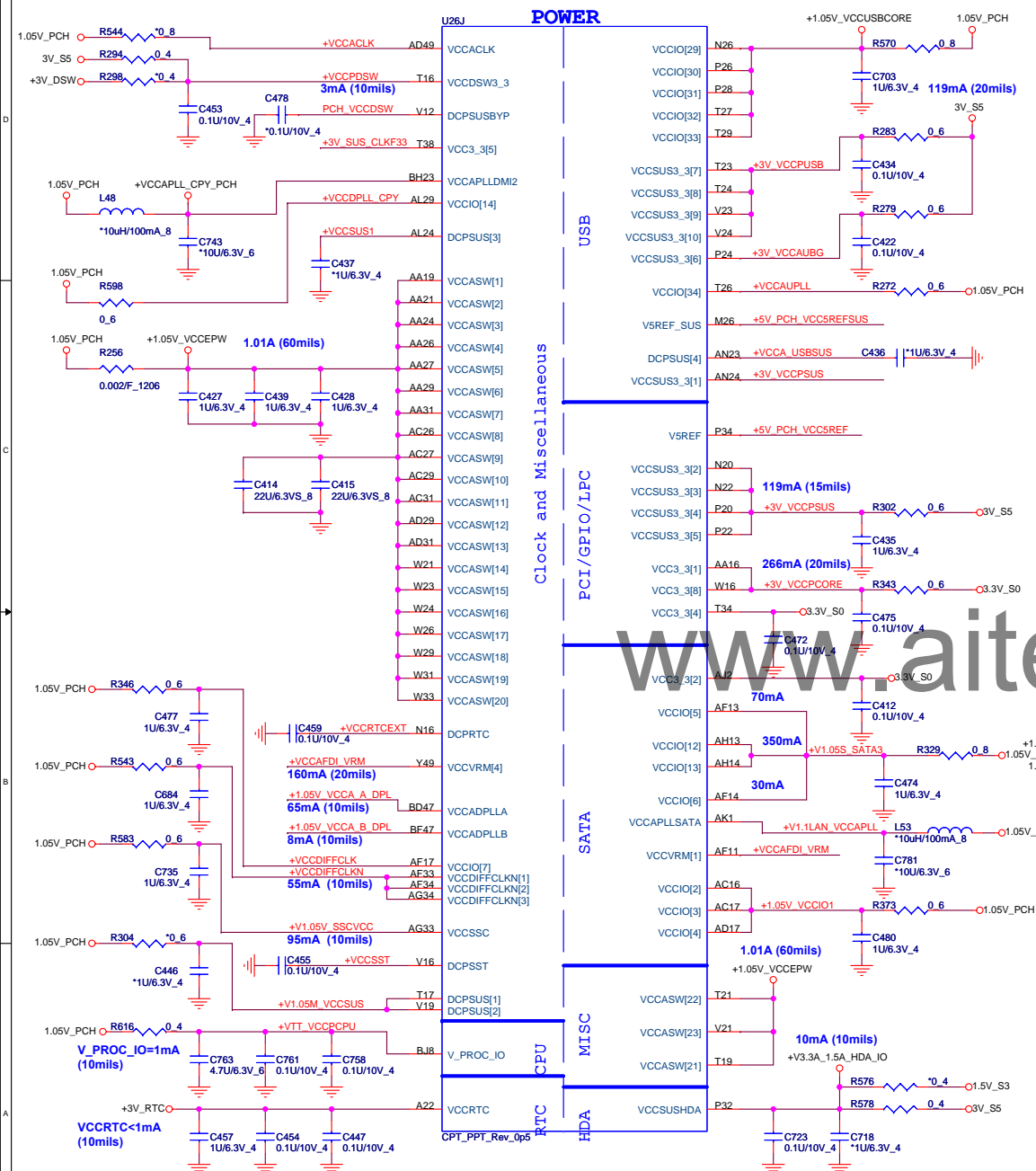




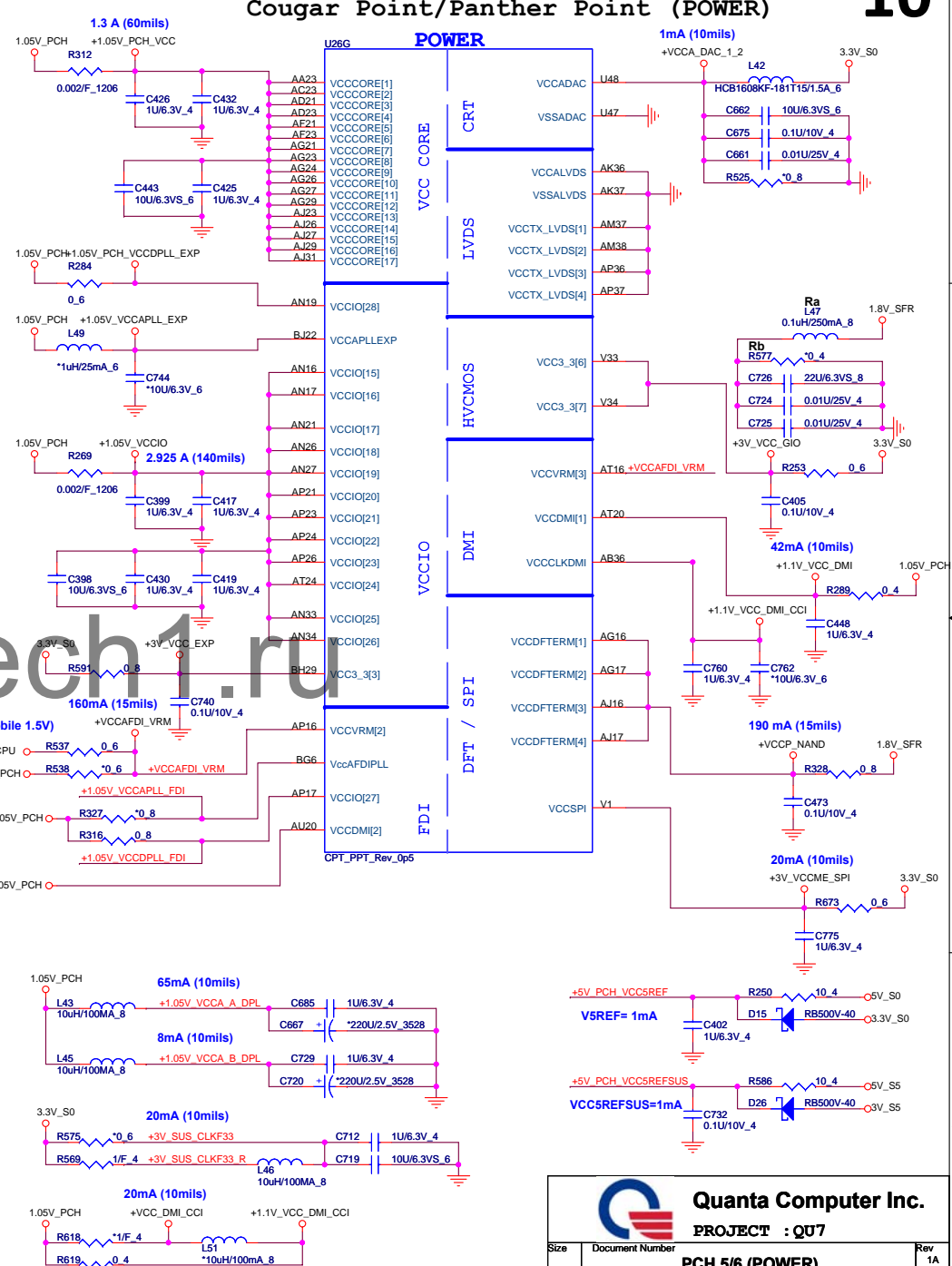




Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (POWER)



## Cougar Point/Panther Point (GND)

U26I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K28
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] P16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P30
BC32	VSS[187]	VSS[287] N47
BC36	VSS[188]	VSS[288] P11
BC34	VSS[189]	VSS[289] P18
BC36	VSS[190]	VSS[290] T33
BC40	VSS[191]	VSS[291] P40
BC42	VSS[192]	VSS[292] P43
BC48	VSS[193]	VSS[293] P47
BD46	VSS[194]	VSS[294] P7
BD5	VSS[195]	VSS[295] R2
BE22	VSS[196]	VSS[296] R48
BE26	VSS[197]	VSS[297] T12
BE40	VSS[198]	VSS[298] T31
BE10	VSS[199]	VSS[299] T37
BE12	VSS[200]	VSS[300] T4
BE16	VSS[201]	VSS[301] W34
BE20	VSS[202]	VSS[302] T46
BE22	VSS[203]	VSS[303] T47
BE24	VSS[204]	VSS[304] T8
BE26	VSS[205]	VSS[305] V11
BD3	VSS[206]	VSS[306] V17
BF30	VSS[207]	VSS[307] V26
BF38	VSS[208]	VSS[308] V27
BF40	VSS[209]	VSS[309] V29
BF8	VSS[210]	VSS[310] V31
BG17	VSS[211]	VSS[311] V36
BG21	VSS[212]	VSS[312] V38
BG33	VSS[213]	VSS[313] V45
BG44	VSS[214]	VSS[314] W7
BG8	VSS[215]	VSS[315] W17
BH11	VSS[216]	VSS[316] W19
BH15	VSS[217]	VSS[317] W2
BH17	VSS[218]	VSS[318] W27
BH19	VSS[219]	VSS[319] W48
H10	VSS[220]	VSS[320] Y12
BH27	VSS[221]	VSS[321] Y38
BH31	VSS[222]	VSS[322] Y4
BH33	VSS[223]	VSS[323] Y42
BH35	VSS[224]	VSS[324] Y46
BH39	VSS[225]	VSS[325] Y8
BH43	VSS[226]	VSS[326] BG29
BH7	VSS[227]	VSS[327] AJ3
D3	VSS[228]	VSS[328] AD47
D12	VSS[229]	VSS[329] B43
D16	VSS[230]	VSS[330] AH11
D18	VSS[231]	VSS[331] AH3
D22	VSS[232]	VSS[332] AH36
D24	VSS[233]	VSS[333] B43
D26	VSS[234]	VSS[334] BE10
D30	VSS[235]	VSS[335] AH42
D32	VSS[236]	VSS[336] AH46
D34	VSS[237]	VSS[337] AH7
D38	VSS[238]	VSS[338] AJ19
D42	VSS[239]	VSS[339] T36
D8	VSS[240]	VSS[340] BG22
E18	VSS[241]	VSS[341] BG24
E26	VSS[242]	VSS[342] C22
G18	VSS[243]	VSS[343] AP13
G20	VSS[244]	VSS[344] M14
G26	VSS[245]	VSS[345] AP3
G28	VSS[246]	VSS[346] AP1
G48	VSS[247]	VSS[347] BE16
H12	VSS[248]	VSS[348] BC16
H18	VSS[249]	VSS[349] BG28
H22	VSS[250]	VSS[350] BJ28
H24	VSS[251]	VSS[351]
H26	VSS[252]	VSS[352]
H30	VSS[253]	
H32	VSS[254]	
H34	VSS[255]	
F3	VSS[256]	
F3	VSS[257]	
F3	VSS[258]	

CPT\_PPT\_Rev\_0p5

## Cougar Point/Panther Point (GND)

U26H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL33
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL48
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AC48	VSS[19]	VSS[98] AM36
AD10	VSS[20]	VSS[99] AM39
AD11	VSS[21]	VSS[100] AM43
AD12	VSS[22]	VSS[101] AM45
AD13	VSS[23]	VSS[102] AM46
AD19	VSS[24]	VSS[103] AM7
AD24	VSS[25]	VSS[104] AN2
AD26	VSS[26]	VSS[105] AN29
AD27	VSS[27]	VSS[106] AN3
AD33	VSS[28]	VSS[107] AN31
AD34	VSS[29]	VSS[108] AP12
AD36	VSS[30]	VSS[109] AP19
AD37	VSS[31]	VSS[110] AP28
AD38	VSS[32]	VSS[111] AP29
AD39	VSS[33]	VSS[112] AP32
AD4	VSS[34]	VSS[113] AP38
AD40	VSS[35]	VSS[114] AP4
AD42	VSS[36]	VSS[115] AP42
AD43	VSS[37]	VSS[116] AP46
AD45	VSS[38]	VSS[117] AP8
AD46	VSS[39]	VSS[118] AR2
AD8	VSS[40]	VSS[119] AR48
AE2	VSS[41]	VSS[120] AT11
AE3	VSS[42]	VSS[121] AT18
AE10	VSS[43]	VSS[122] AT22
AE12	VSS[44]	VSS[123] AT26
AD14	VSS[45]	VSS[124] AT28
AD16	VSS[46]	VSS[125] AT30
AE16	VSS[47]	VSS[126] AT32
AF19	VSS[48]	VSS[127] AT34
AF24	VSS[49]	VSS[128] AT39
AF26	VSS[50]	VSS[129] AT42
AF27	VSS[51]	VSS[130] AT46
AF3	VSS[52]	VSS[131] AT7
AF38	VSS[53]	VSS[132] AU24
AF4	VSS[54]	VSS[133] AU30
AF42	VSS[55]	VSS[134] AV16
AF46	VSS[56]	VSS[135] AV20
AF5	VSS[57]	VSS[136] AV24
AF7	VSS[58]	VSS[137] AV30
AF8	VSS[59]	VSS[138] AV38
AG19	VSS[60]	VSS[139] AV4
AG2	VSS[61]	VSS[140] AV43
AG31	VSS[62]	VSS[141] AV8
AG33	VSS[63]	VSS[142] AW14
AG48	VSS[64]	VSS[143] AW18
AN24	VSS[65]	VSS[144] AW22
AH11	VSS[66]	VSS[145] AW28
AH36	VSS[67]	VSS[146] AW32
AH39	VSS[68]	VSS[147] AW34
BE10	VSS[69]	VSS[148] AW36
AH42	VSS[70]	VSS[149] AW40
AH46	VSS[71]	VSS[150] AW48
AH7	VSS[72]	VSS[151] AV11
AJ19	VSS[73]	VSS[152] AY12
AJ21	VSS[74]	VSS[153] AY22
AJ24	VSS[75]	VSS[154] AY28
AJ33	VSS[76]	VSS[155]
AJ34	VSS[77]	VSS[156]
AJ4	VSS[78]	VSS[157]
AK12	VSS[79]	VSS[158]
AK3		

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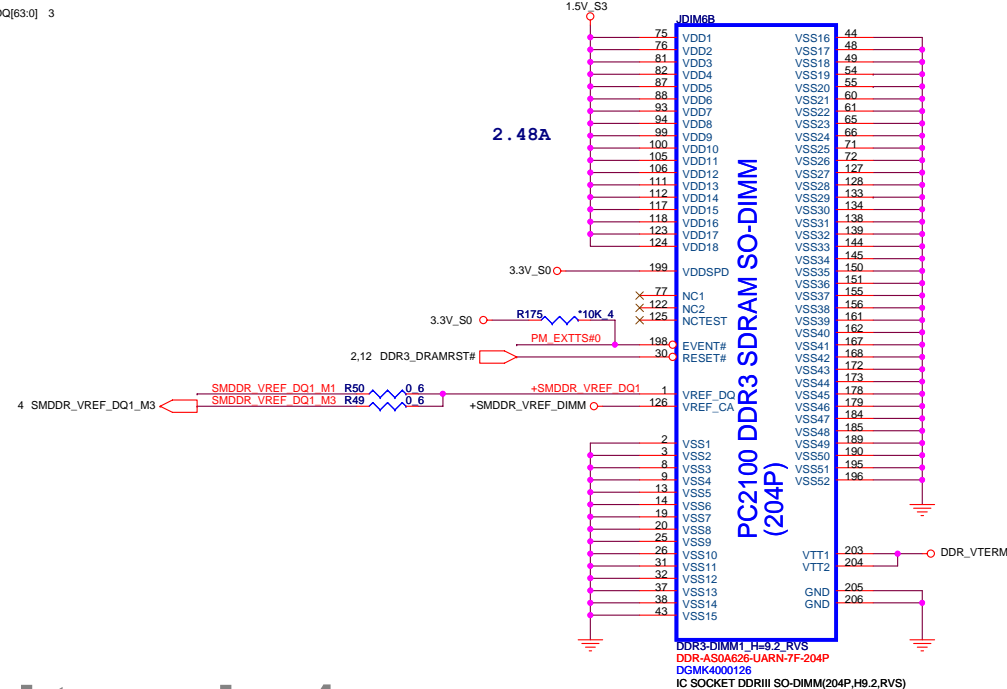
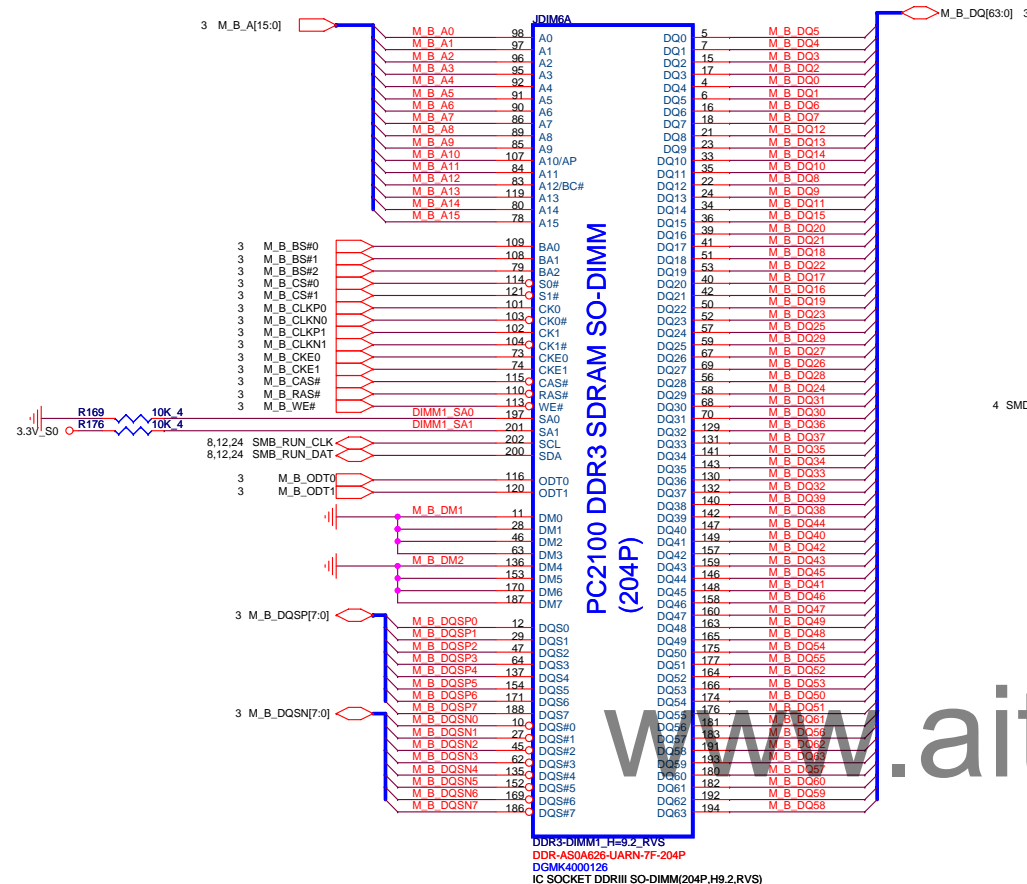
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			1A

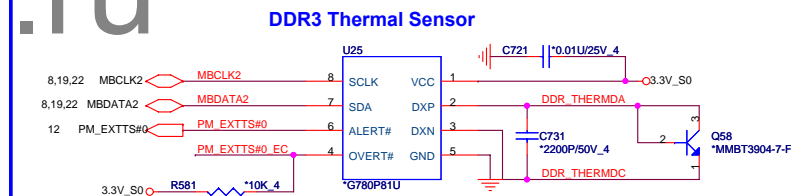
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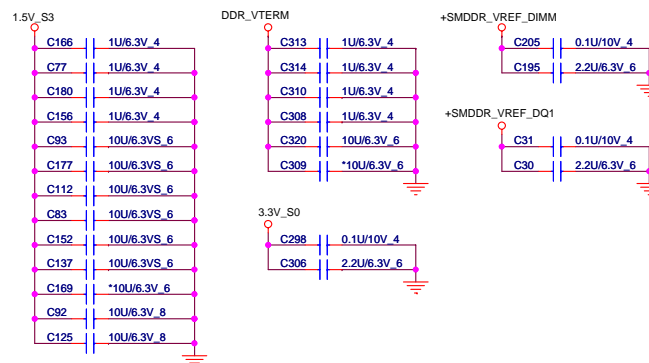
 **Quanta Computer Inc.**  
PROJECT : QU7



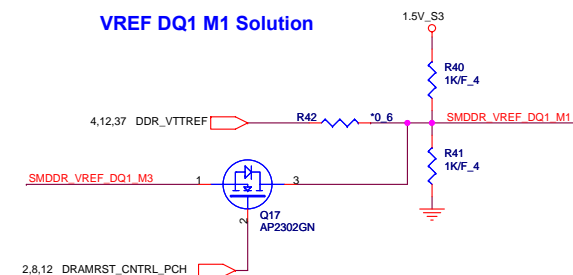
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### Place these Caps near So-Dimm1.

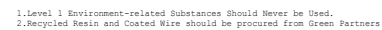


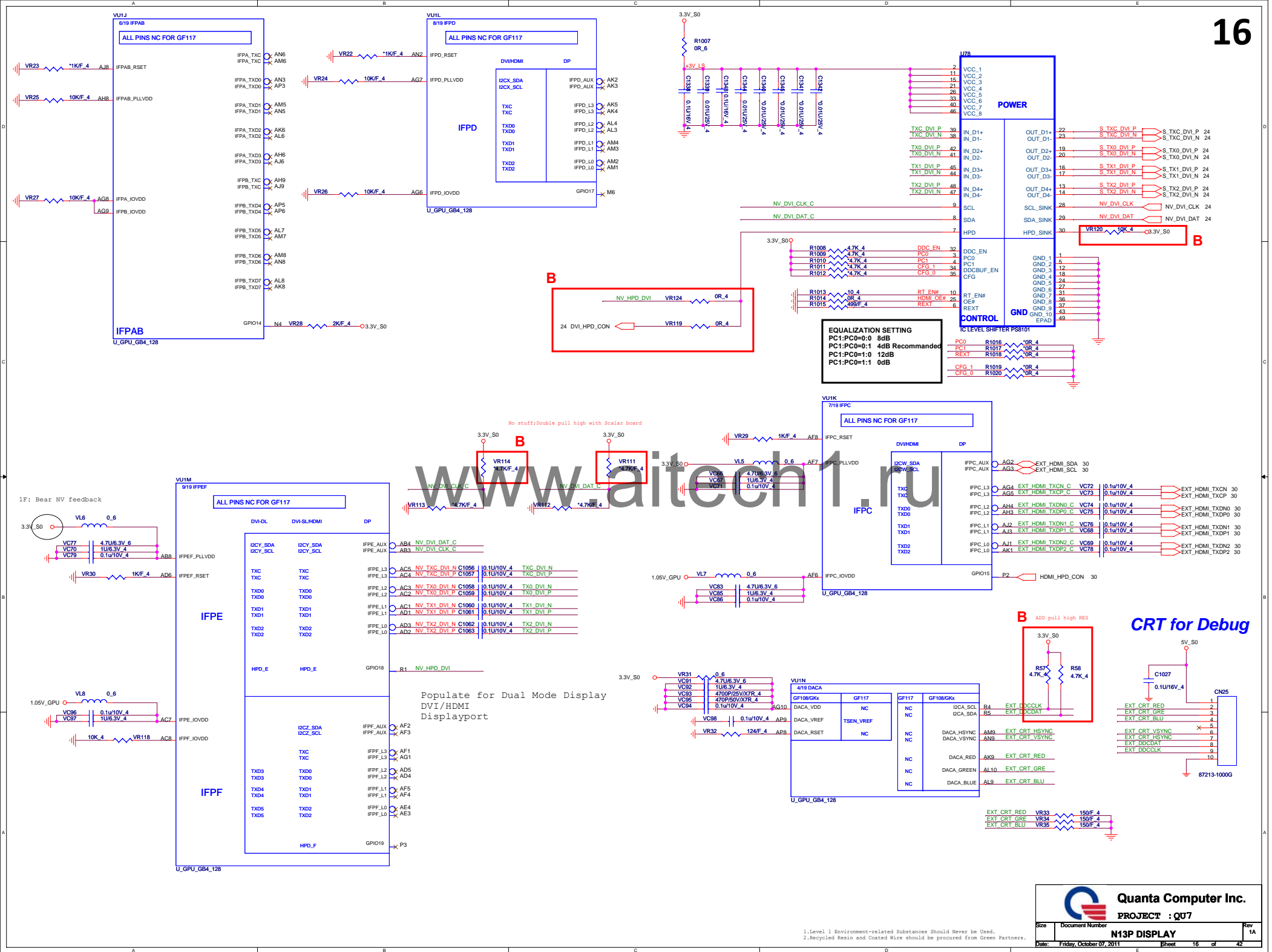
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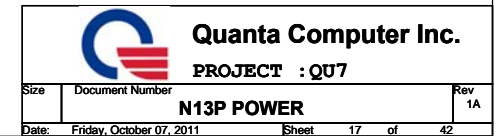




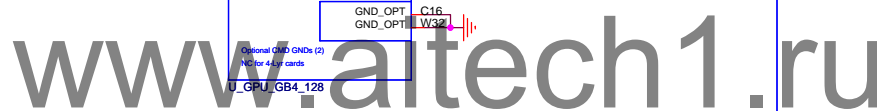




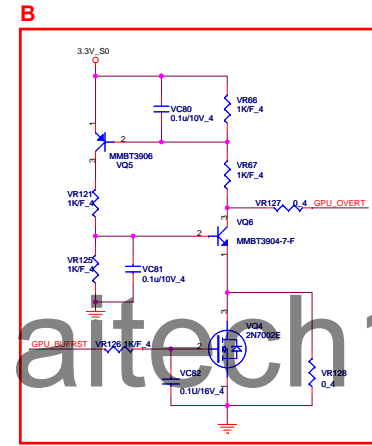
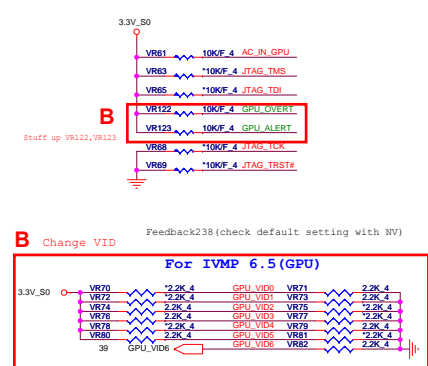
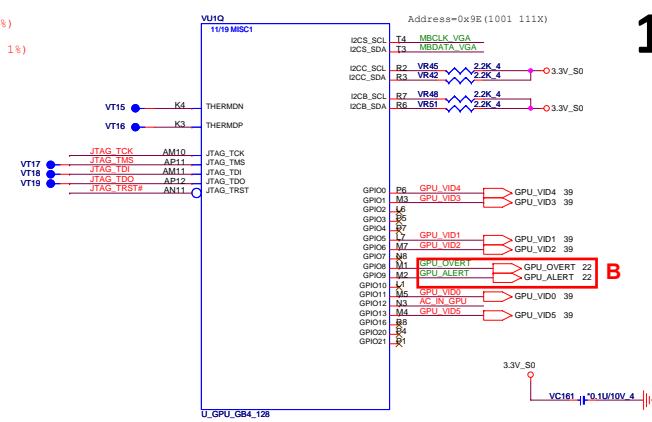
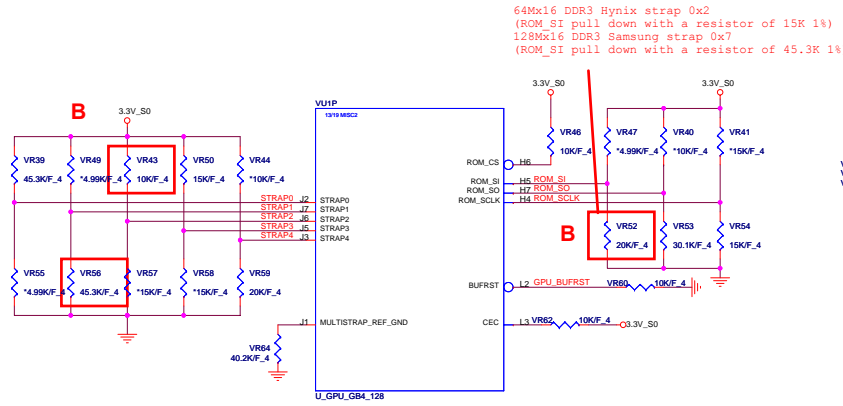




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	<b>N13P POWER</b>	1A
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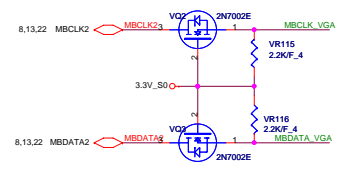
Logical Strap Bit Mapping			
	PU-VDD	PD	QC1 PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB26
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

VRAM(DDR3) Configuration Table						
RAMCFG [3:0]	DESCRIPTION (Vendor P/N)	Vendor	QCI P/N	ROM_SI	ET SMT	
0010	64*16-900MHz	H5TG1G63DFR-11C	Hynix	AKDLS2TW2	PD 15K	X
0011	64*16-900MHz	K4W1G1646C-BC11	Samsung	AK8BEGGT500	PD 20K	O
0110	128*16-900MHz	H5TQ2G63BFR-11C	Hynix	Reverse	PD 34.8K	X
0111	128*16-900MHz	K4W2G1646C-HC11	Samsung	Reverse	PD 45.3K	X

N13P-GS/GLP	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417 FB[1]	FB_0_BAR_SIZE FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG PCI_DEVIDE[5]	PEX_PLL_EN_TERM	1010
ROM_S1	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD3V	0011
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	1010
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1111 1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

## GPIO ASSIGNMENTS

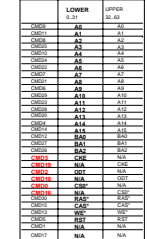
GPIO	I/O	ACTIVE	USAGE
0	<b>OUT</b>	N/A	NVVDD VID4
1	OUT	N/A	NVVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID1
6	OUT	N/A	NVVDD VID2
7	OUT	N/A	3D STEREO
8	I/O	LOW	GPU Overtemp
9	I/O	LOW	GPU ALERT
10	OUT	N/A	FB Vref Control (not used sDDR3)
11	OUT	N/A	NVVDD VID0
12	IN	N/A	PWR_Level AC Detect
13	OUT	N/A	NVVDD VID5
14	IN	N/A	HPD for IFP AB (not used)
15	IN	N/A	HPD for IFP C (HDMI)
16	OUT	N/A	MEM_VDD_CTL
17	OUT	N/A	HPD for IFP D (not used)
18	OUT	N/A	HPD for IFP E (TMDS)
19	OUT	N/A	HPD for IFP F (not used)
20	OUT	N/A	NVGEM Debug GPIO13
21	OUT	N/A	NVGEM Debug GPIO14



ES Samples GS/GLP:15K PU

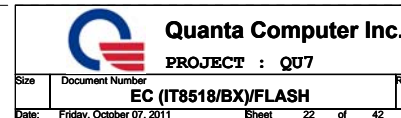
DG\_table111

notebook default  
EDID is used

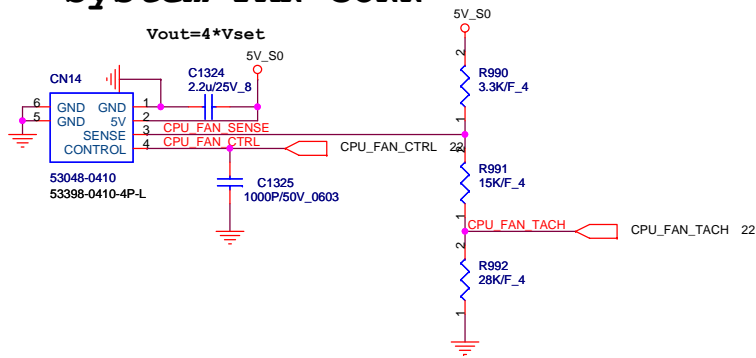


	LOWER	UPPER
CMS00	A0	A0
CMS01	A2	A1
CMS02	A2	A2
CMS03	A2	A3
CMS04	A3	A4
CMS05	A5	A5
CMS06	A6	A6
CMS07	A7	A7
CMS08	A8	A8
CMS09	A9	A9
CMS10	A10	A10
CMS11	A11	A11
CMS12	A12	A12
CMS13	A13	A13
CMS14	A14	A14
CMS15	A15	A15
CMS16	B00	B00
CMS17	B01	B01
CMS18	B02	B02
CMS19	C00	C00
CMS20	D00	D00
CMS21	E00	E00
CMS22	F00	F00
CMS23	G00	G00
CMS24	H00	H00
CMS25	I00	I00
CMS26	J00	J00
CMS27	K00	K00
CMS28	L00	L00
CMS29	M00	M00
CMS30	N00	N00
CMS31	O00	O00
CMS32	P00	P00
CMS33	Q00	Q00
CMS34	R00	R00
CMS35	S00	S00
CMS36	T00	T00
CMS37	U00	U00
CMS38	V00	V00
CMS39	W00	W00
CMS40	X00	X00
CMS41	Y00	Y00
CMS42	Z00	Z00
CMS43	AA	AA
CMS44	AB	AB
CMS45	AC	AC
CMS46	AD	AD
CMS47	AE	AE
CMS48	AF	AF
CMS49	AG	AG
CMS50	AH	AH
CMS51	AI	AI
CMS52	AM	AM
CMS53	AN	AN
CMS54	AO	AO
CMS55	AP	AP
CMS56	AQ	AQ
CMS57	AR	AR
CMS58	AS	AS
CMS59	AT	AT
CMS60	AV	AV
CMS61	AW	AW
CMS62	AX	AX
CMS63	AY	AY
CMS64	BA	BA
CMS65	BB	BB
CMS66	BC	BC
CMS67	BD	BD
CMS68	BE	BE
CMS69	BF	BF
CMS70	BG	BG
CMS71	BH	BH
CMS72	BI	BI
CMS73	BJ	BJ
CMS74	BK	BK
CMS75	BL	BL
CMS76	BM	BM
CMS77	BN	BN
CMS78	BO	BO
CMS79	BP	BP
CMS80	BQ	BQ
CMS81	BR	BR
CMS82	BS	BS
CMS83	BT	BT
CMS84	BU	BU
CMS85	BV	BV
CMS86	BW	BW
CMS87	BX	BX
CMS88	BY	BY
CMS89	BZ	BZ
CMS90	CA	CA
CMS91	CB	CB
CMS92	CC	CC
CMS93	CD	CD
CMS94	CE	CE
CMS95	CF	CF
CMS96	CG	CG
CMS97	CH	CH
CMS98	CI	CI
CMS99	CJ	CJ
CMS100	CK	CK
CMS101	CL	CL
CMS102	CM	CM
CMS103	CN	CN
CMS104	CO	CO
CMS105	CP	CP
CMS106	CQ	CQ
CMS107	CR	CR
CMS108	CS	CS
CMS109	CT	CT
CMS110	CU	CU
CMS111	CV	CV
CMS112	CW	CW
CMS113	CX	CX
CMS114	CY	CY
CMS115	CZ	CZ
CMS116	DA	DA
CMS117	DB	DB
CMS118	DC	DC
CMS119	DD	DD
CMS120	DE	DE
CMS121	DF	DF
CMS122	DG	DG
CMS123	DH	DH
CMS124	DI	DI
CMS125	DJ	DJ
CMS126	DK	DK
CMS127	DL	DL
CMS128	DM	DM
CMS129	DN	DN
CMS130	DO	DO
CMS131	DP	DP
CMS132	DQ	DQ
CMS133	DR	DR
CMS134	DS	DS
CMS135	DT	DT
CMS136	DU	DU
CMS137	DV	DV
CMS138	DW	DW
CMS139	DX	DX
CMS140	DY	DY
CMS141	DZ	DZ
CMS142	EA	EA
CMS143	EB	EB
CMS144	EC	EC
CMS145	ED	ED
CMS146	EE	EE
CMS147	EF	EF
CMS148	EG	EG
CMS149	EH	EH
CMS150	EI	EI
CMS		

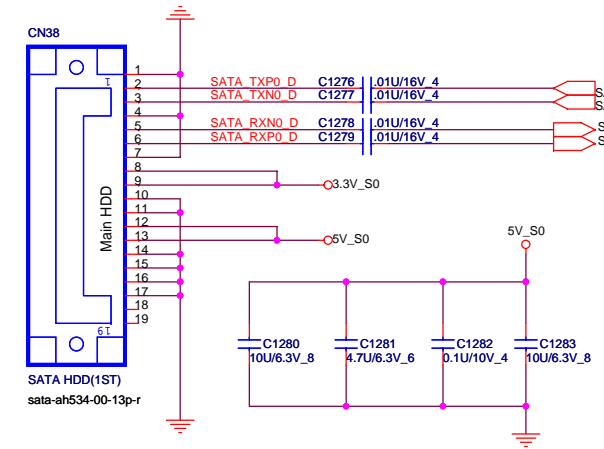




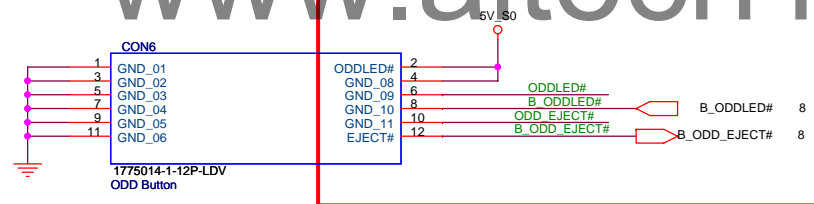
# System FAN CONN



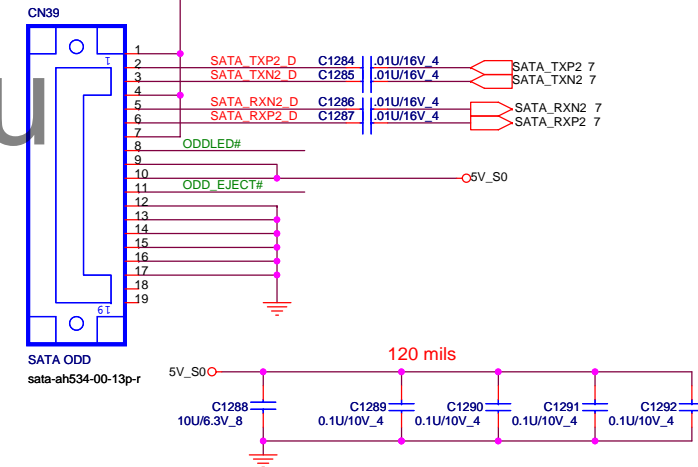
# SATA HDD CONN



# ODD BUTTON BTB CONN

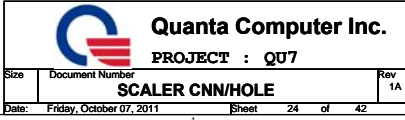


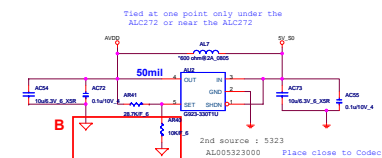
# SATA ODD CONN



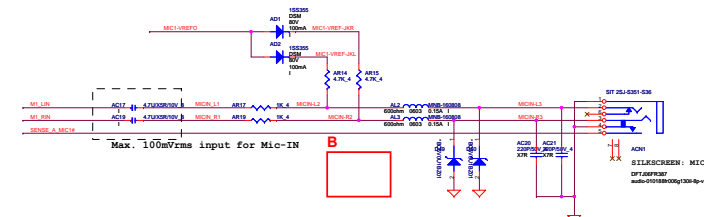


24

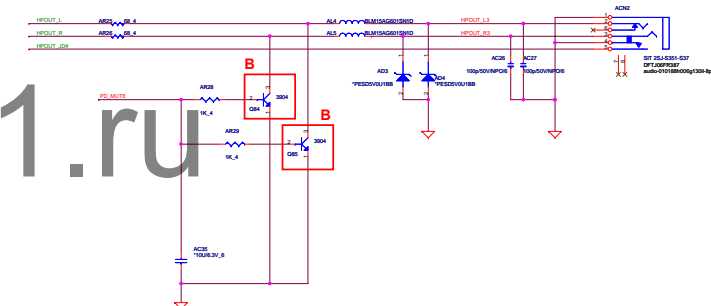




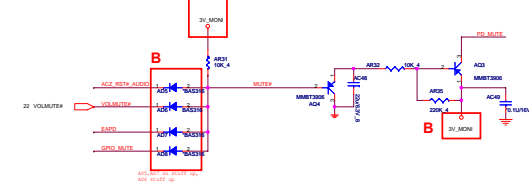
## SYSTEM MIC



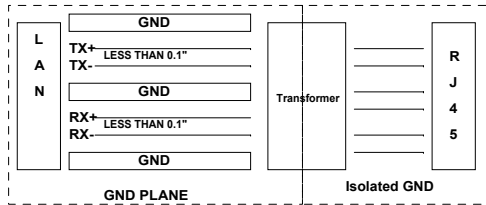
## Head Phone



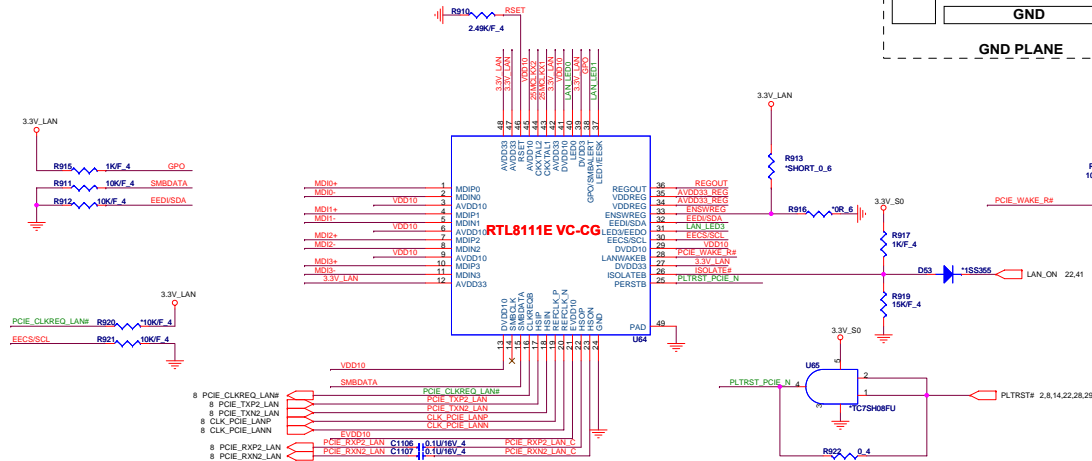
**MUTE**



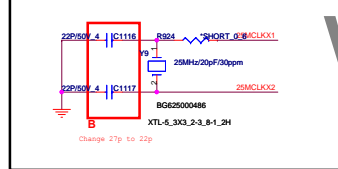
TX 100 ohm ---> trace 4 mil , space 7 mil  
 RX 50 mil space from other signals  
 Total Trace Length no more than 4"  
 2 Differential pairs must have the same length



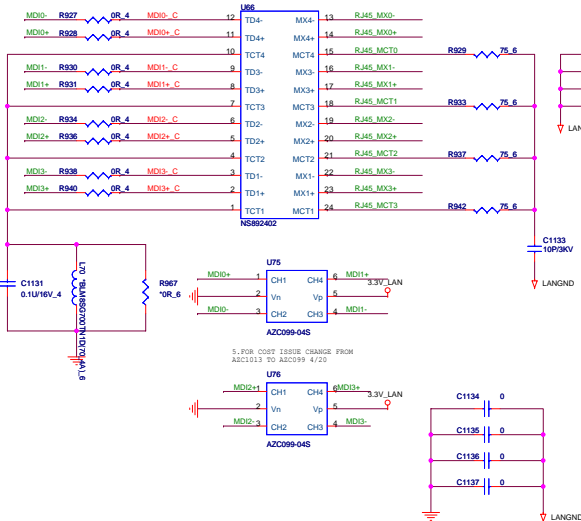
## RTL8111F



## X'tal 25MHz

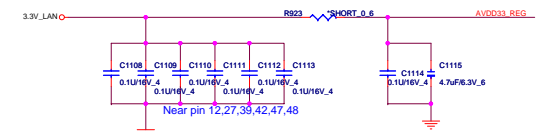


## LAN Transformer

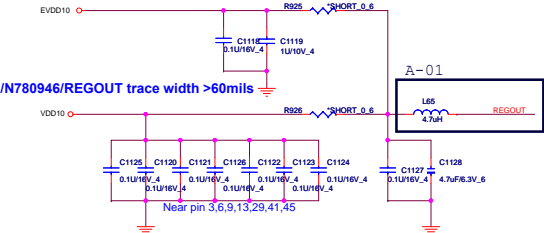


## LAN POWER

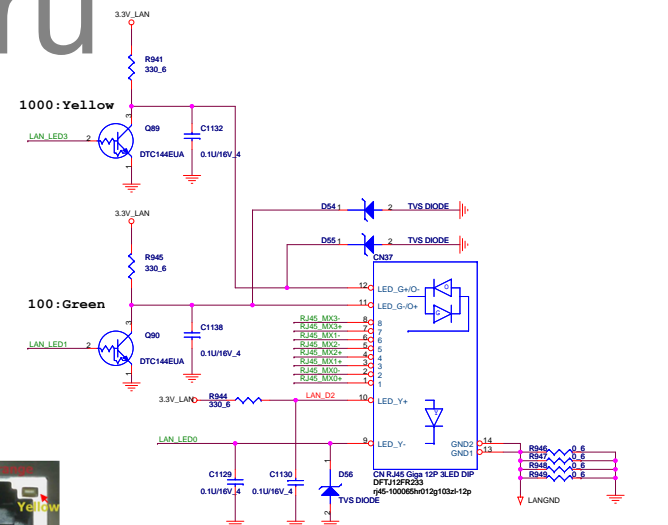
EVDD10/AVDD33\_REG trace width &gt;60mils



EVDD10 trace width &gt;60mils

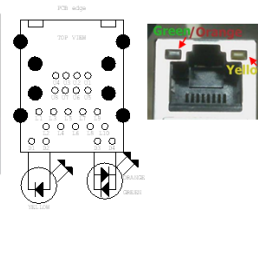
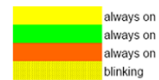


EVDD10/N780946/REGOUT trace width &gt;60mils

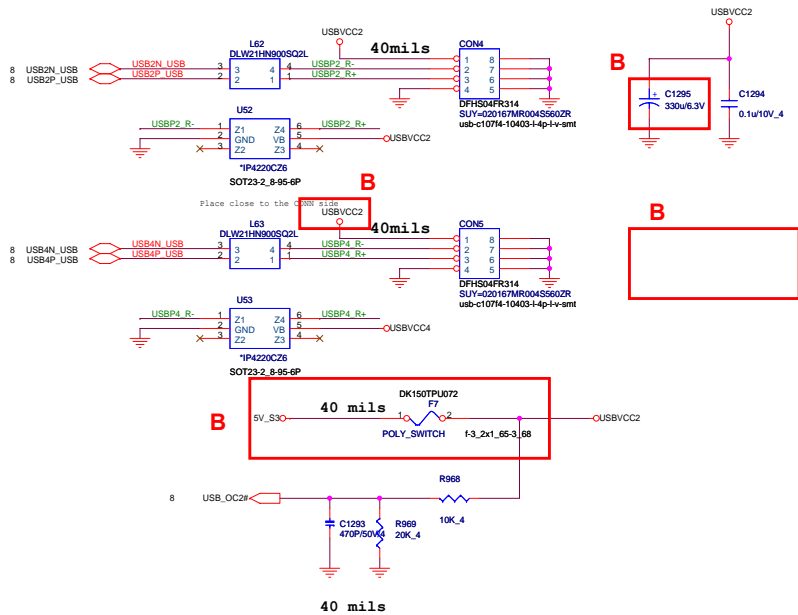


## 9.1. Lan Connector requirement.

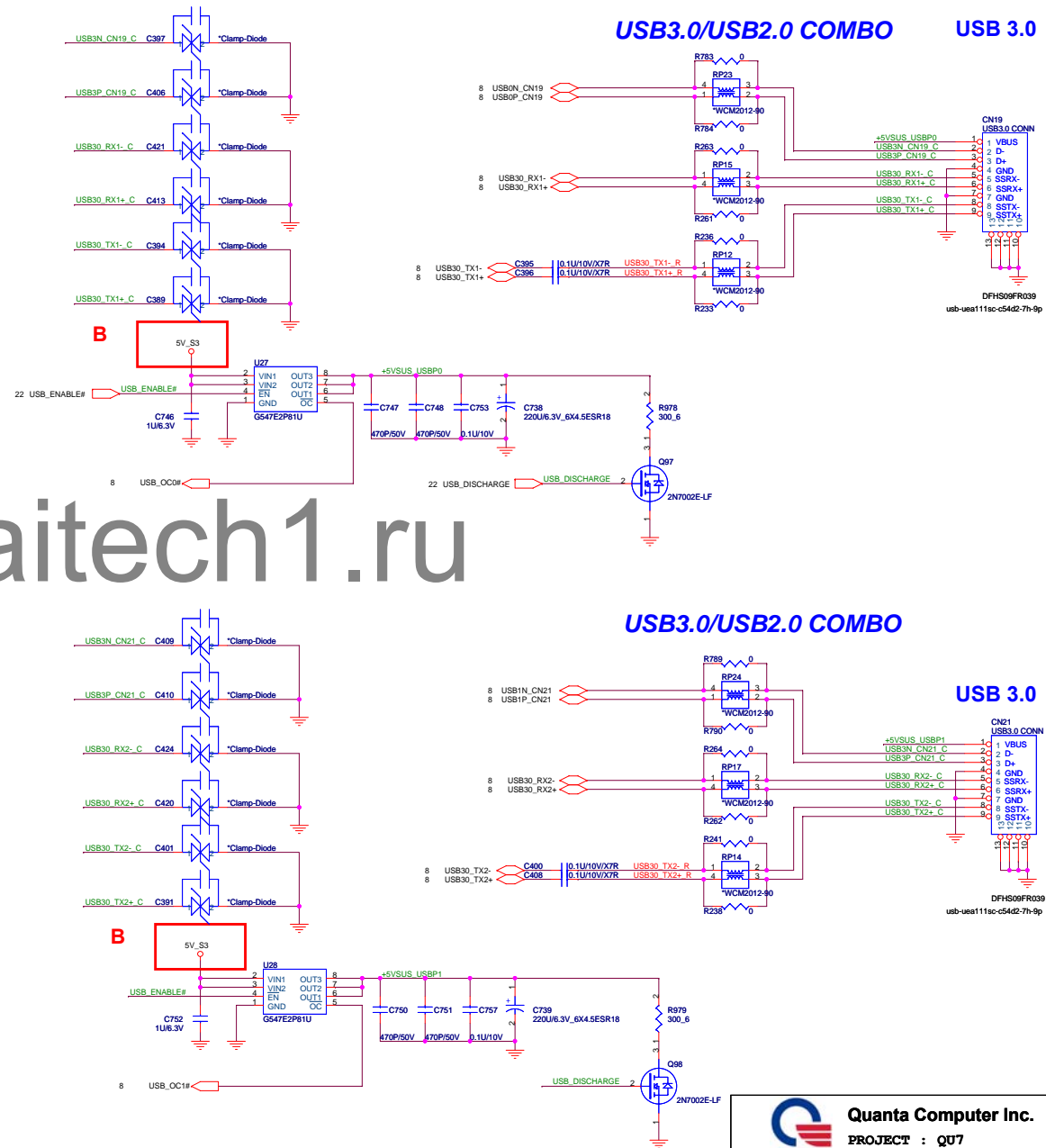
WOL	status	Yellow	Gm/Org
don't care	No Link	off	off
on	WOL	off	off
on	10M inactive	off	off
on	10M active	off	off
on	100M inactive	off	off
on	100M active	off	off
on	1G inactive	off	off
on	1G active	off	off



# USB2.0 CNN

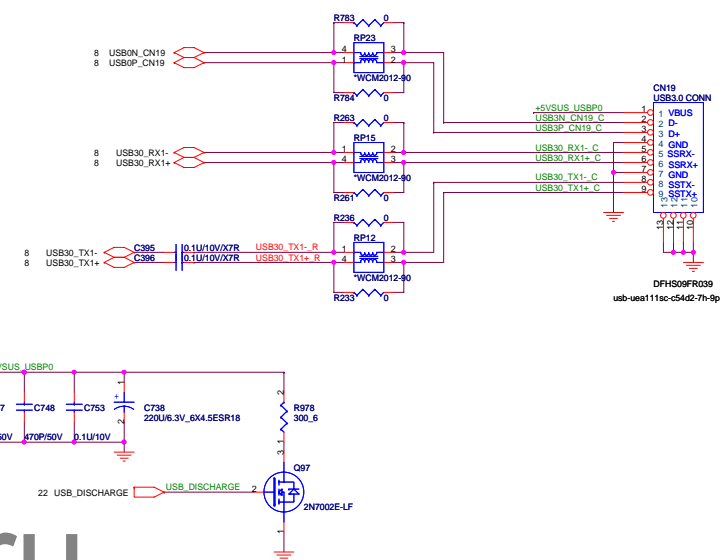


# USB3.0 CNN



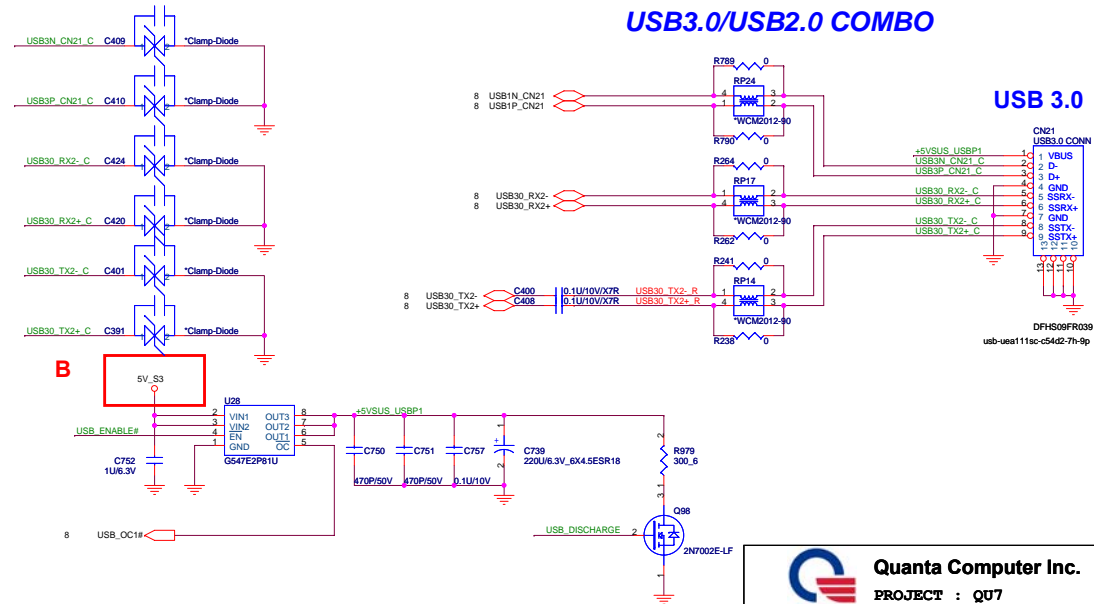
## USB3.0/USB2.0 COMBO

## USB 3.0

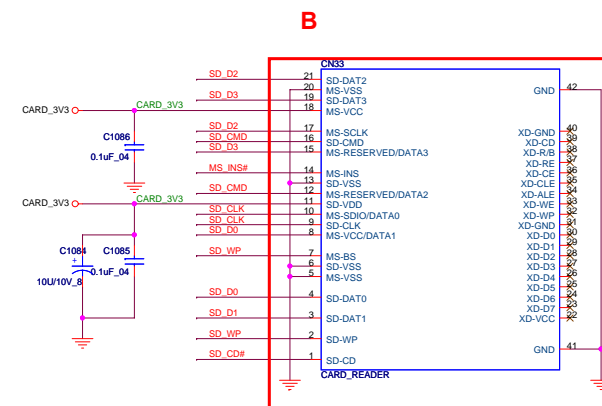
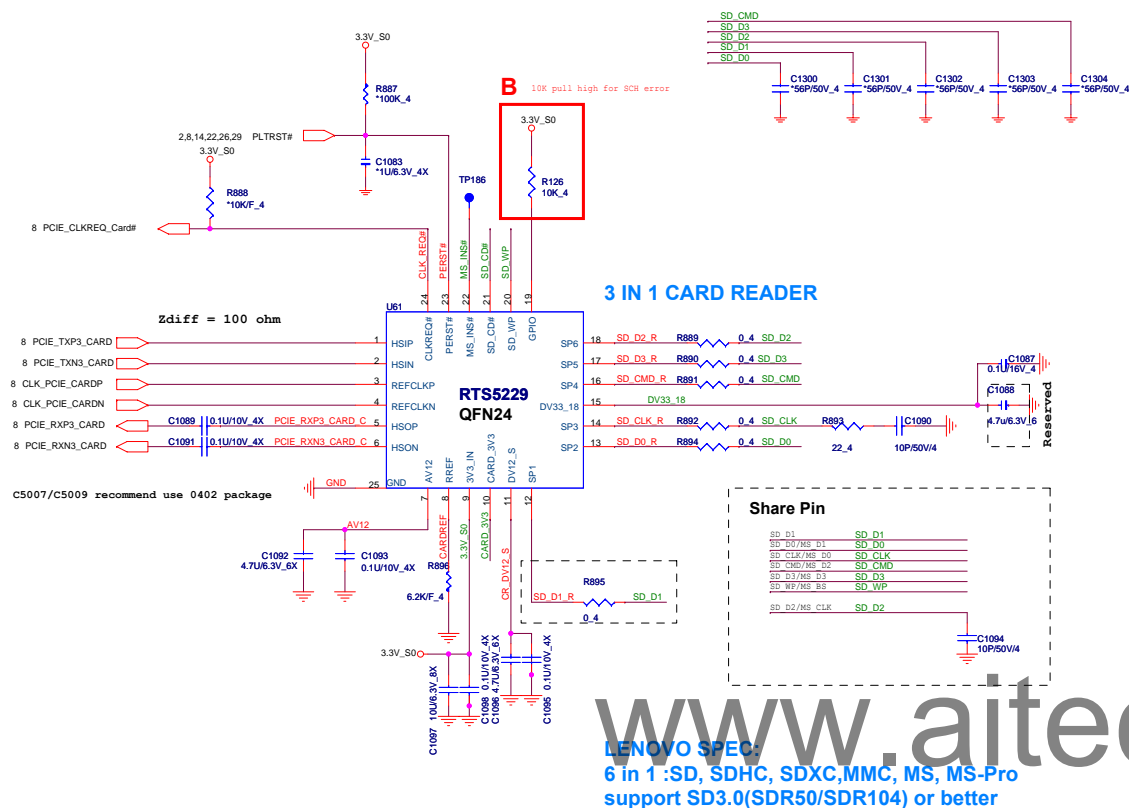


## USB3.0/USB2.0 COMBO

## USB 3.0



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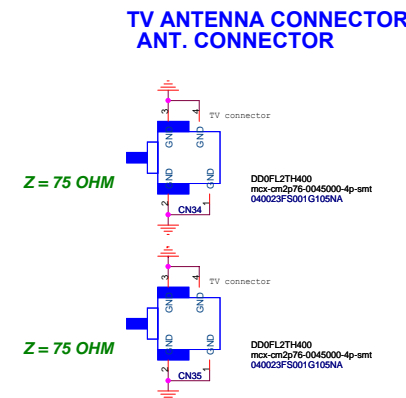


Share Pin

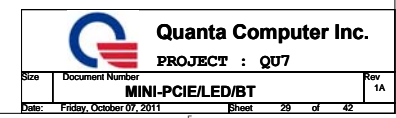
Share Pin	XD	MS	SD
SP1			SD_D1
SP2		MS_D1	SD_D0
SP3		MS_D0	SD_CLK
SP4		MS_D2	SD_CMD
SP5		MS_D3	SD_D3
SP6		MS_CLK	SD_D2
SP7		MS_BS	

**LENOVO SPEC:**  
6 in 1 :SD, SDHC, SDXC,MMC, MS, MS-Pro  
support SD3.0(SDR50/SDR104) or better

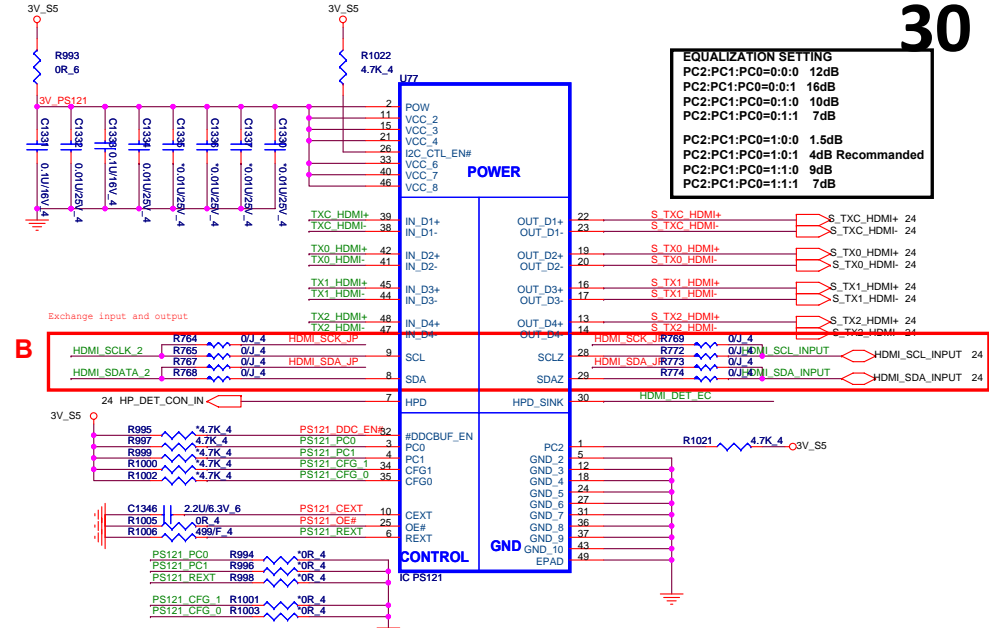
29



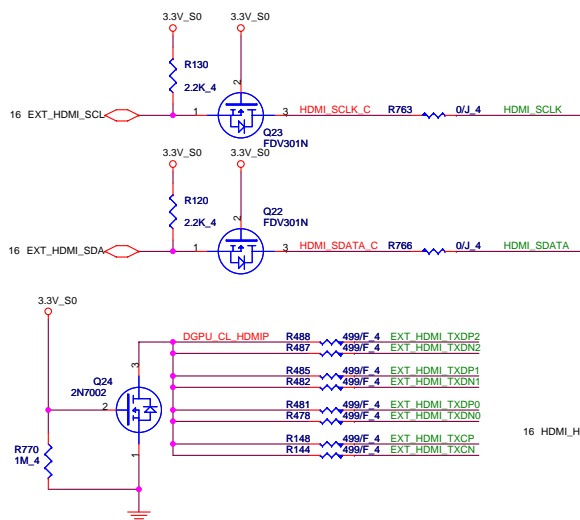
## Mini Card-mSATA



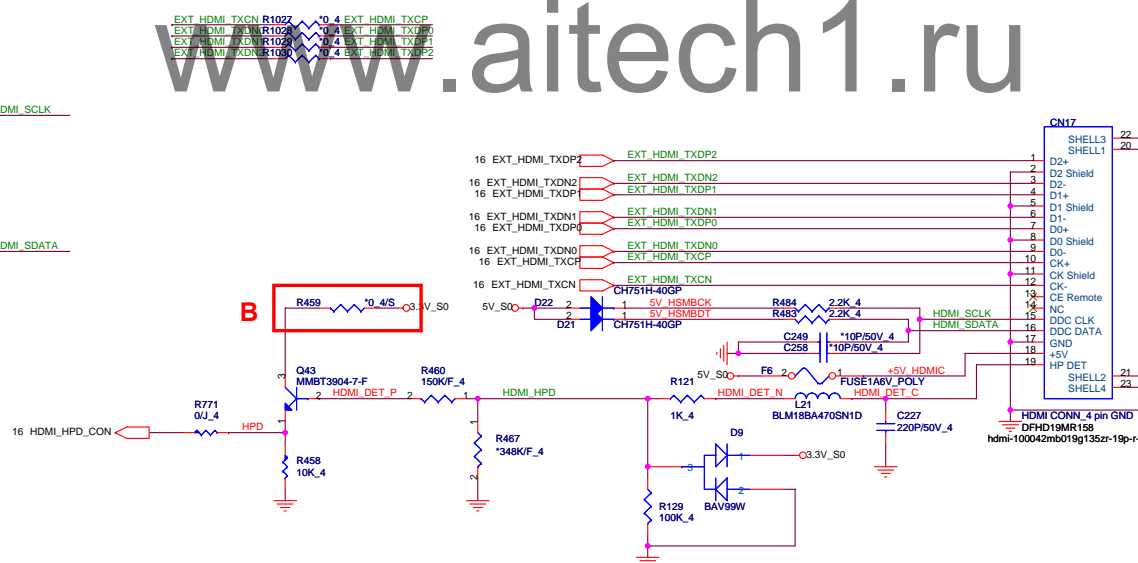
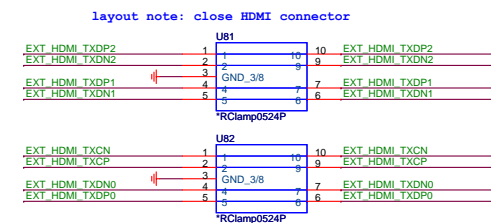


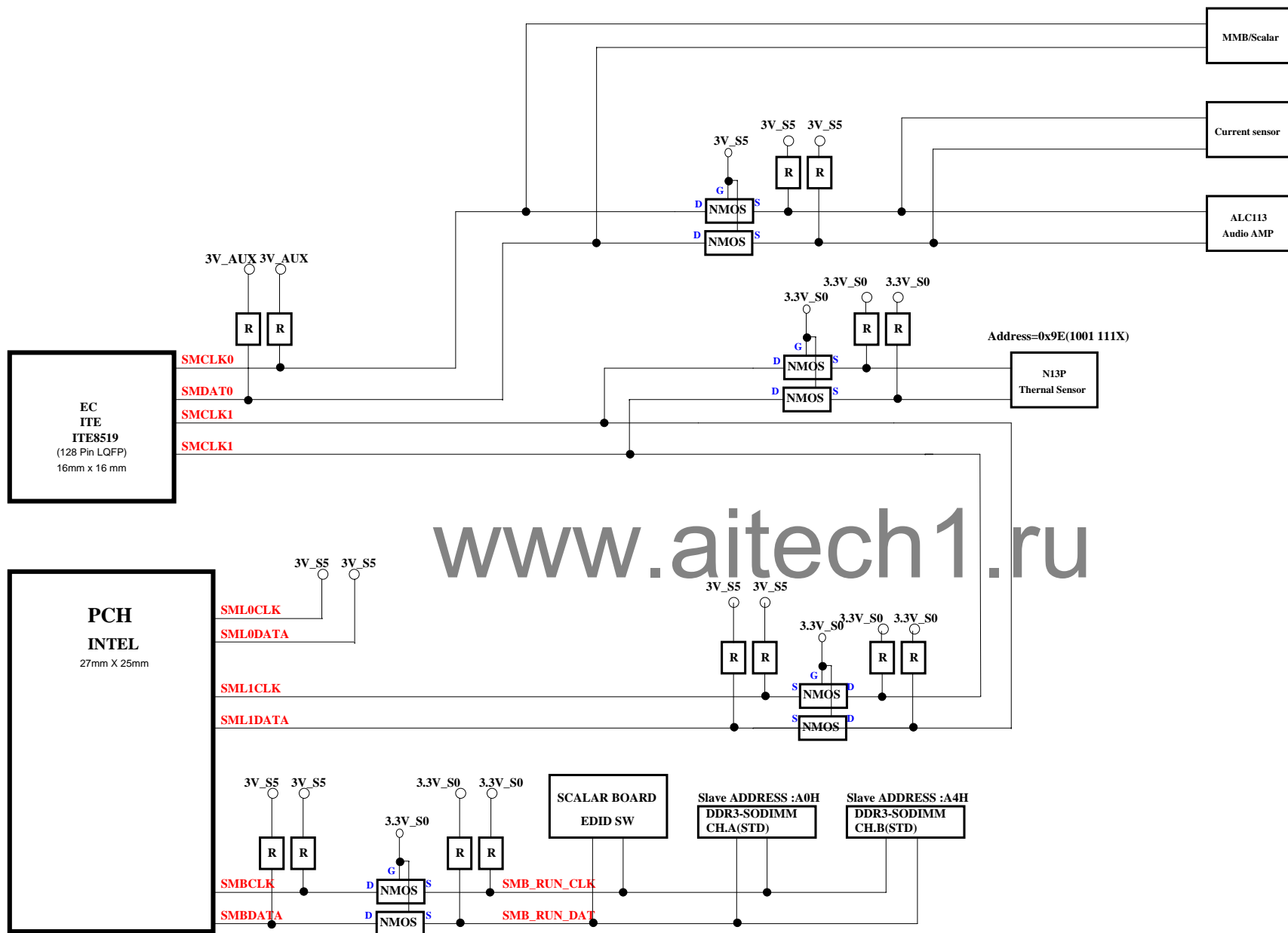


## HDMI-OUT PORT

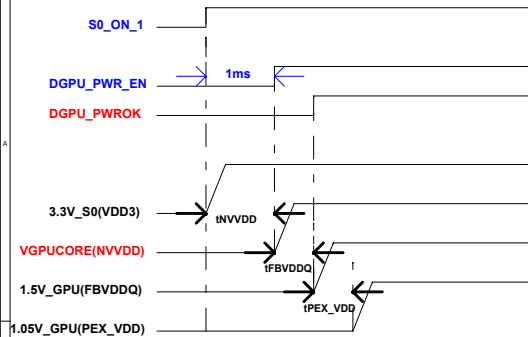


## ESD Protection





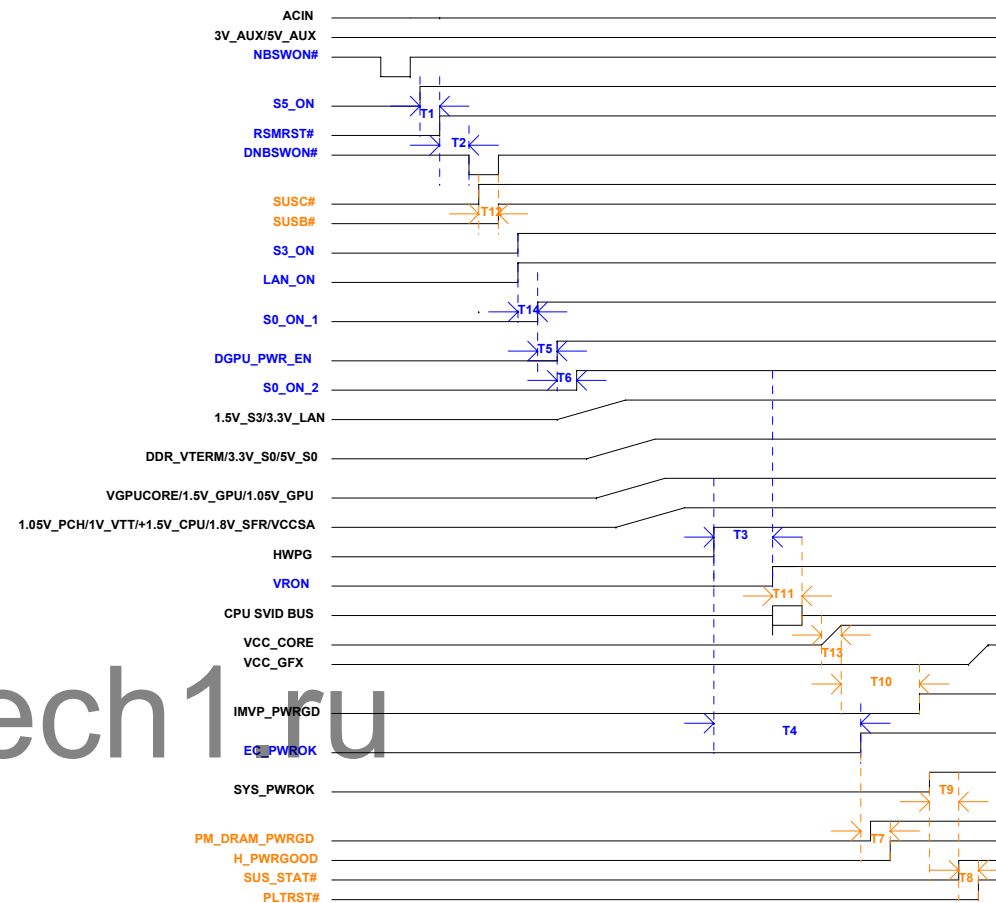
## N13P-x POWER UP SEQUENCE



N13P-x POWER UP SEQUENCE  
 tINVDD>0  
 tFBVDDQ>0  
 tPEX\_VDD>0

## QU7 POWER-ON SEQUENCE

32



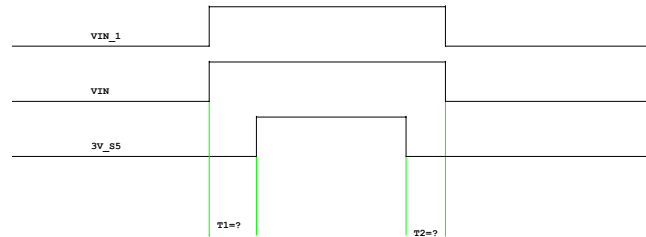
System Power Sequence  
 T1: S5\_ON TO RSMRST# = 30ms (spec:mini 10ms)  
 T2: RSMRST# TO DNBSWON# = 110ms (spec:mini 100ms)  
 T3: HWPG TO VRON = 10ms  
 T4: HWPG TO EC\_PWROK = 99ms (Min)  
 T5: S0\_ON\_1 TO DGPU\_PWR\_EN = 2.1 ms  
 T6: DGPU\_PWR\_EN TO S0\_ON\_2 = 3.2 ms  
 T7: EC\_PWROK TO H\_PWRGOOD = 2ms(Min)  
 T8: SUS\_STAT# TO PLTRST# = 60us(Min)  
 T9: SYS\_PWROK TO SUS\_STAT# = 1ms(Min)  
 T10: VCC\_CORE TO IMVP\_PWRGD = 5ms(Max)  
 T11: VRON to accept SVID command. = 5ms(Max)  
 T12: SUSC# to SUSB# = 30us(Min)  
 T13: VCC\_CORE ramp time = 50-2000us  
 T14: LAN\_ON(S3\_ON) to S0\_ON\_1 = 1ms

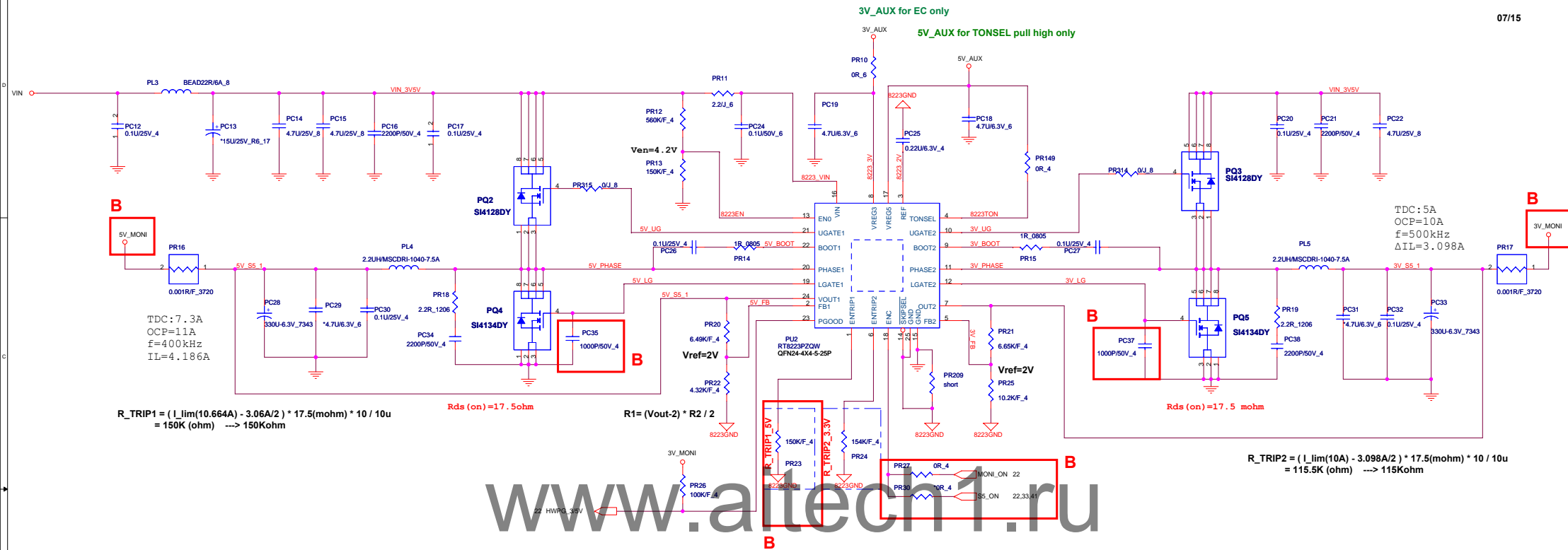
## Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal	Location
+3V_RTC	3V	ON	ON	ON	ON	ON		Mother board
VIN	19.5V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
12V_AUX	12V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
5V_S5	5V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
3V_S5	3V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
1.2V_S5	1.2V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON	Mother board
3.3V_LAN	3V	ON	Note	Note	Note	OFF	LAN_ON	Mother board
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
3.3V_S0	3V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
1.05V_PCH	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
1V_VTT	1V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
VCCSA	By VID	ON	OFF	OFF	OFF	OFF	HWPG_VTT	Mother board
+1.5V_CPU	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
1.8V_SFR	1.8V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
VGPUCORE	By VID	ON	OFF	OFF	OFF	OFF	DGPU_PWR_EN	Mother board
1.5V_GPU	1.5V	ON	OFF	OFF	OFF	OFF	DGPU_PWROK	Mother board
1.05V_GPU	1.05V	ON	OFF	OFF	OFF	OFF	DGPU_PWROK	Mother board
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON	Mother board

Note: Depend on WOL

```
ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms
```





$$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$$

#### O.C.P setup information

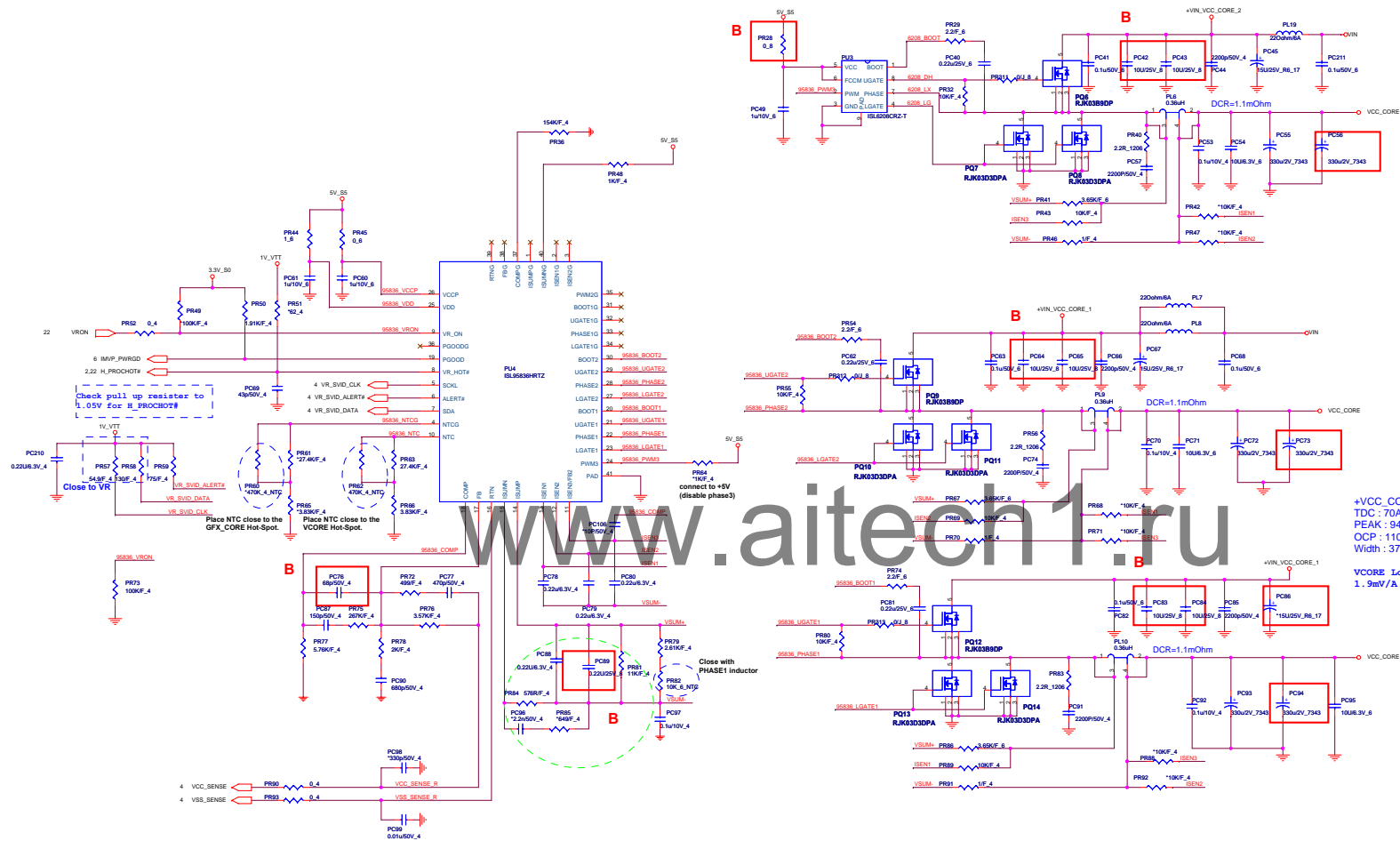
Output	Mos	Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V		17.5m_Max	14.25	4.186	400	2.2uH	150K
3.3V		17.5m_Max	10	3.098	500	2.2uH	115K

#### L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m

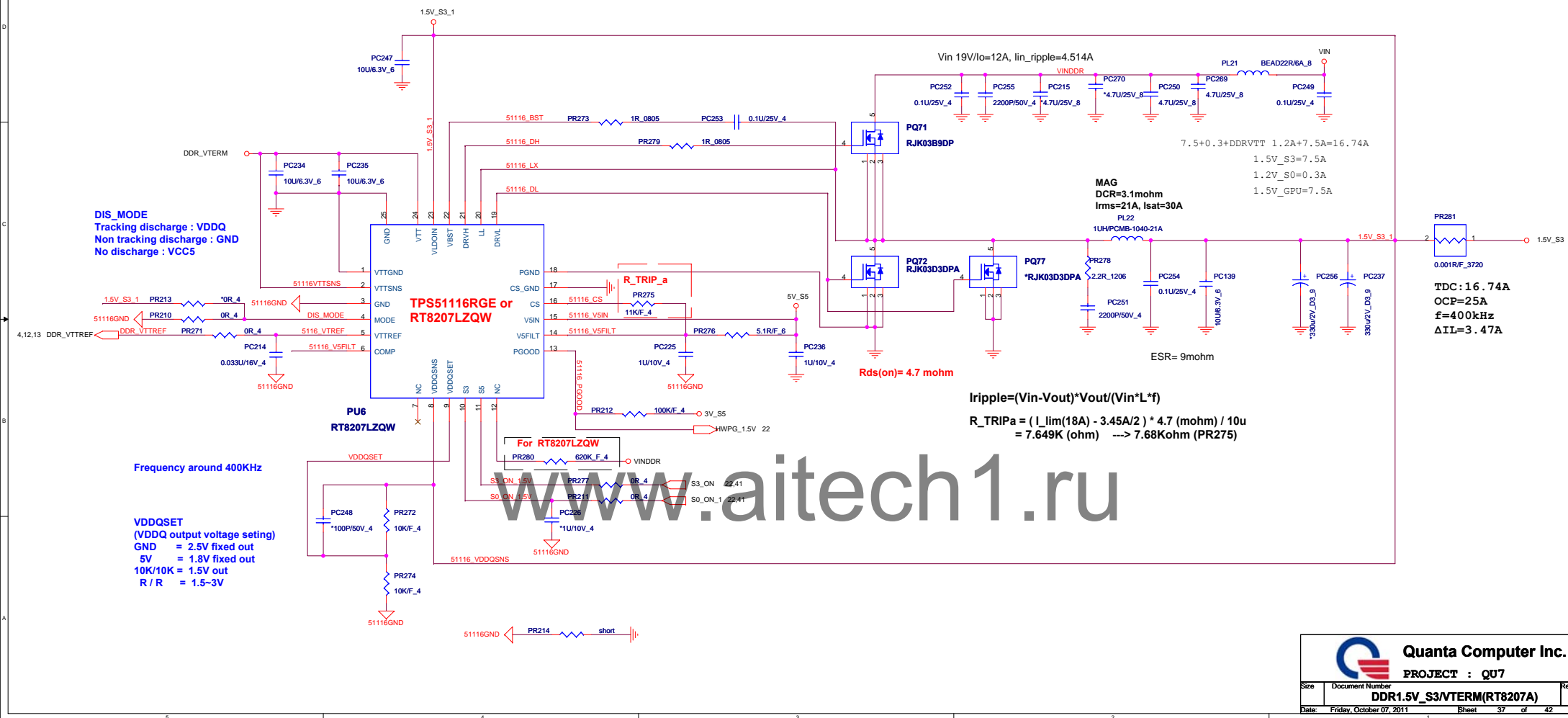
#### Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON





[illegible]

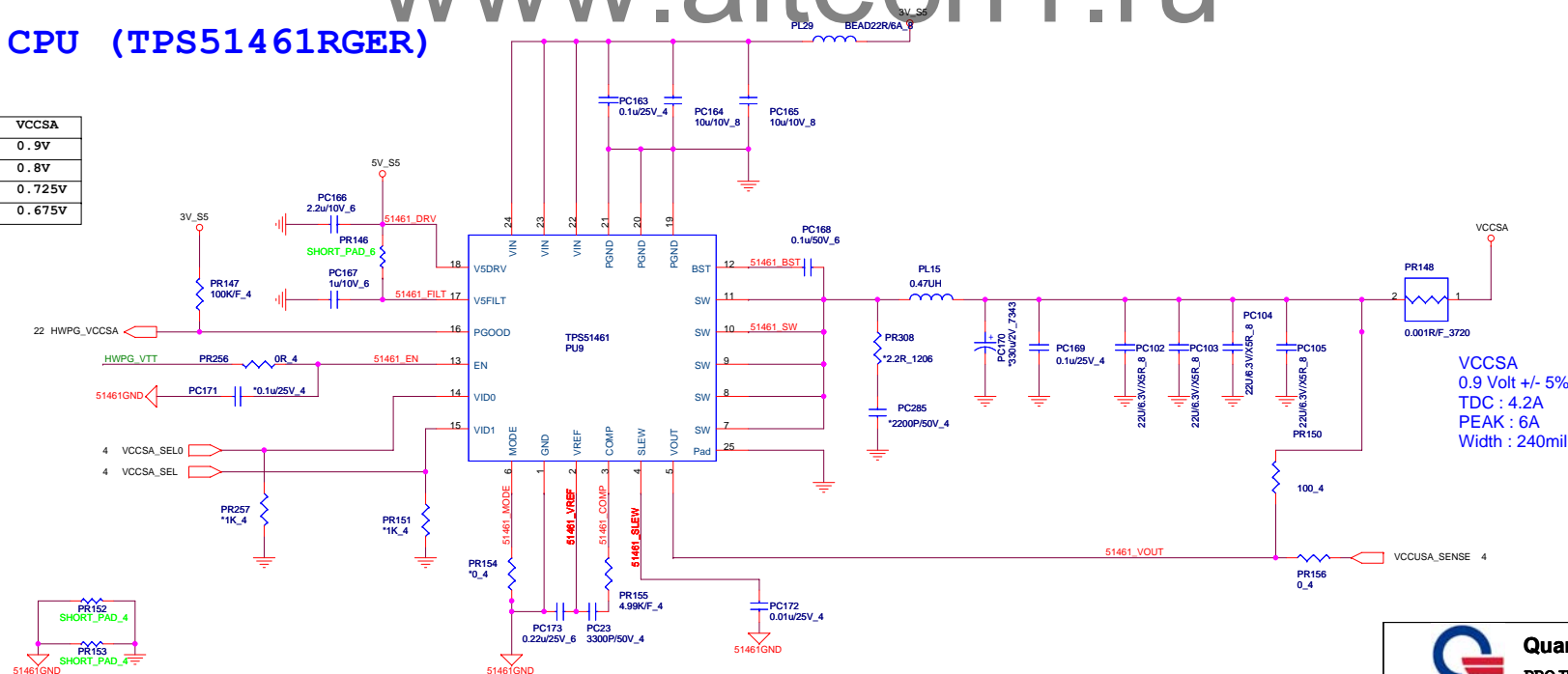




## VCCSA FOR CPU (TPS51461RGER)

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

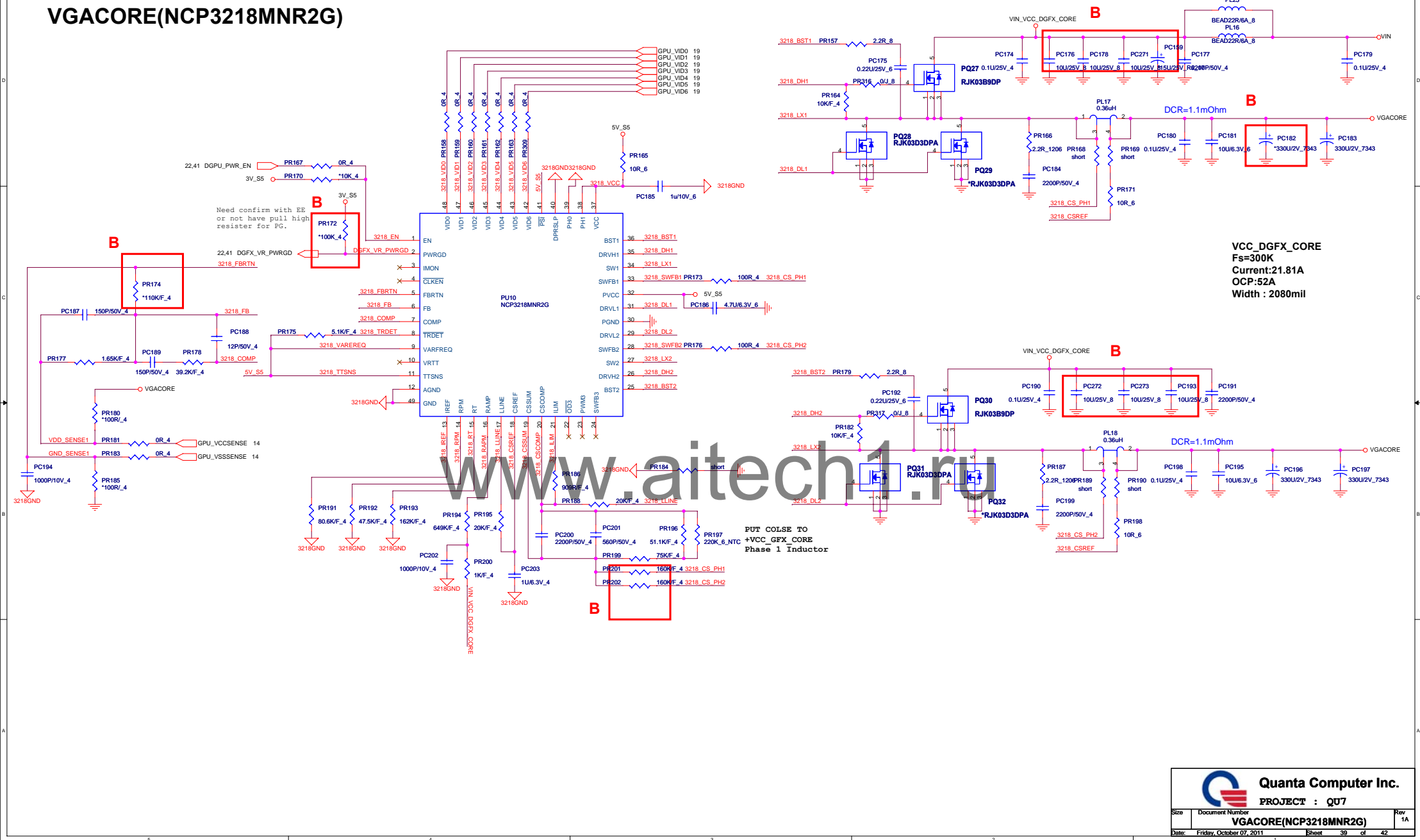
**Quanta Computer Inc.**

**PROJECT : OU7**

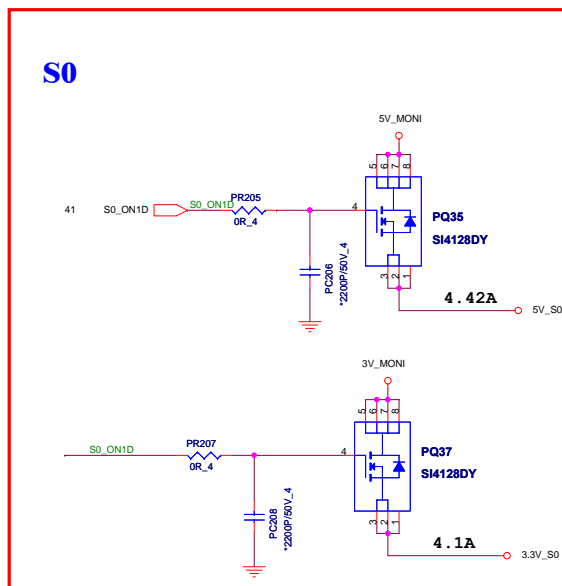
**1V\_VTT/ VCCSA**

Rev	1A
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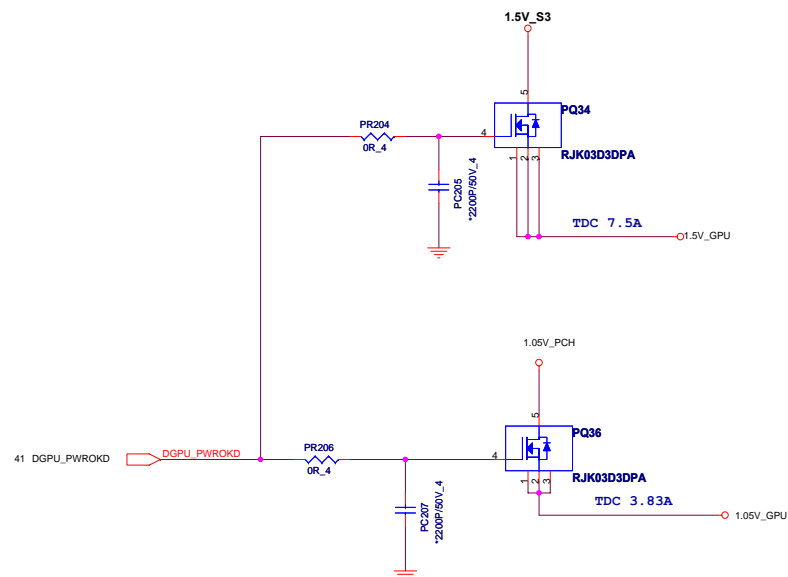
## VGACORE(NCP3218MNR2G)



S0

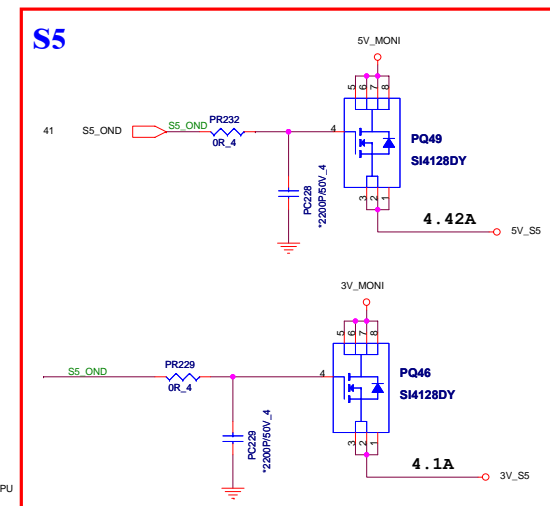


VGA



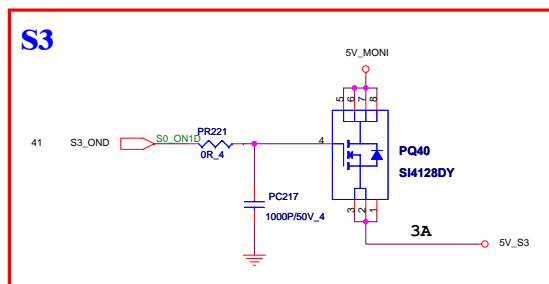
B

S5

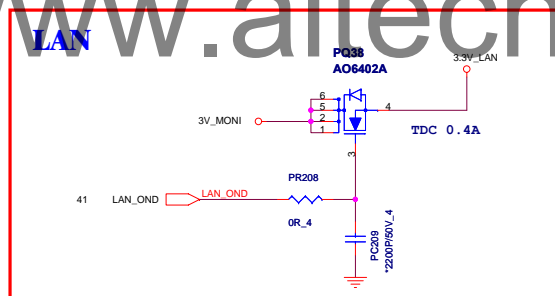


B

S3



LAN



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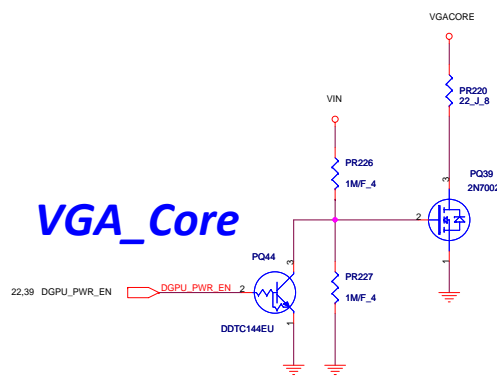


Quanta Computer Inc.

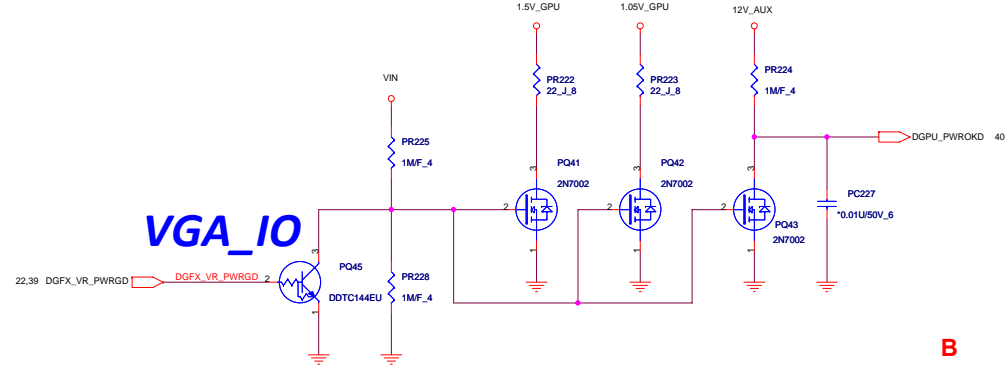
PROJECT : QU7

Size	Document Number	Rev
	LOAD SWITCH	1A
Date: Friday, October 07, 2011	Sheet 40 of 42	

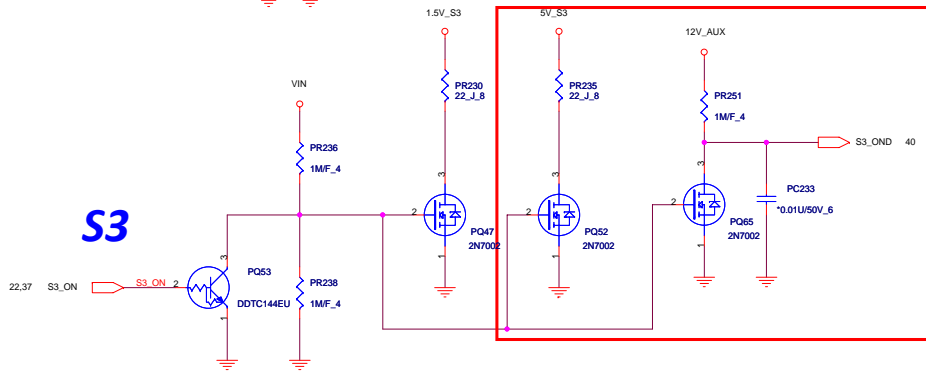
## VGA\_Core



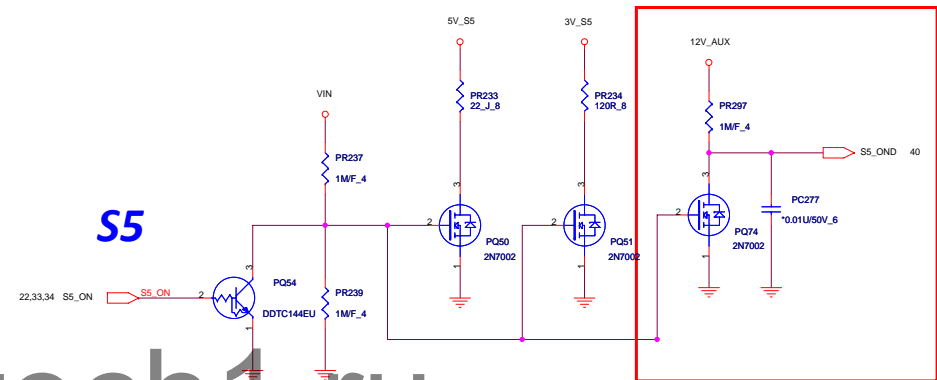
## VGA\_IO



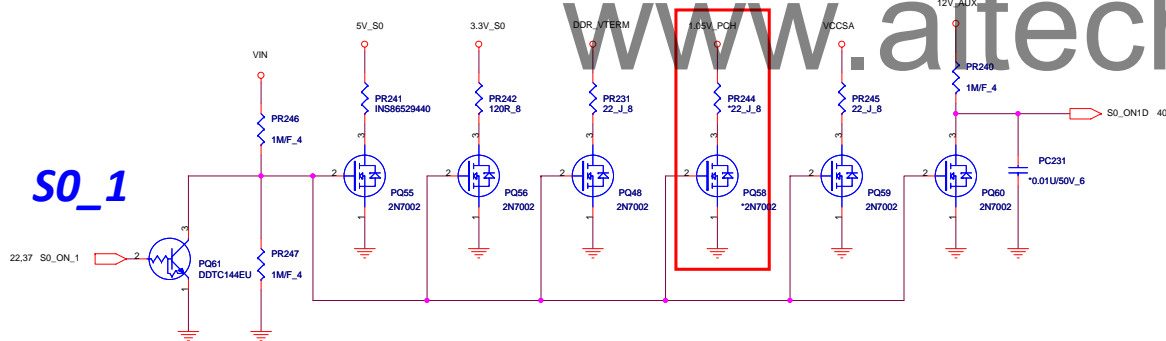
## S3



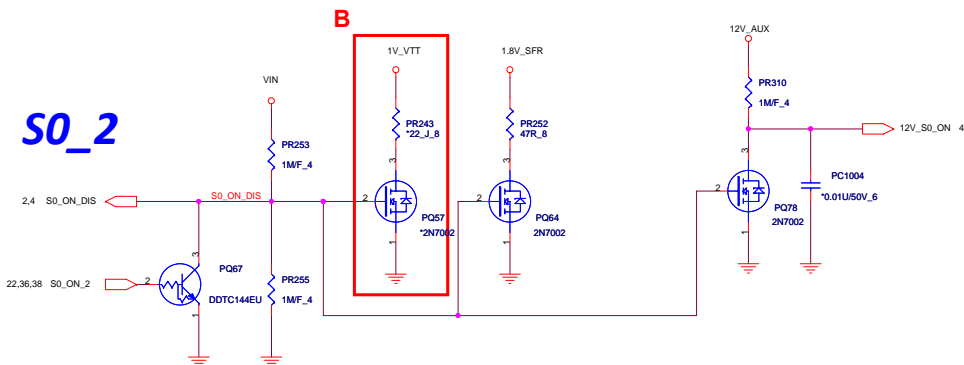
## S5



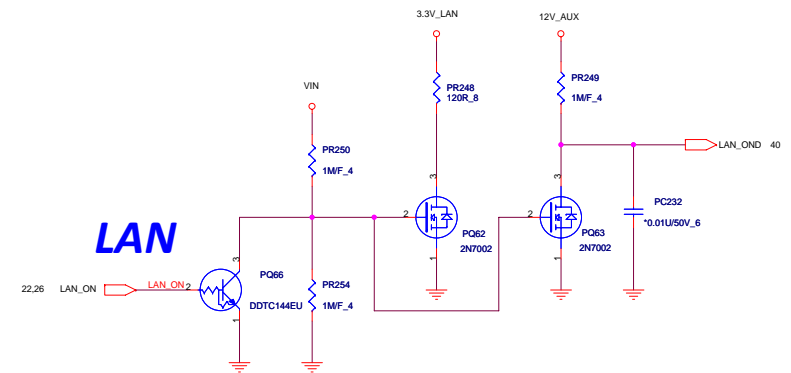
## S0\_1



## S0\_2



## LAN





**A->B**

PAGE22:<1>Add D57 and support awake EC from idle mode

<2>HDMI\_DET\_EC swap PIN with SLP\_SUS#

PAGE24: Add Q99 and control Vin to supply C/B under S0 only.

PAGE30: DEL R459 in BOM. The footprint is shortpad.

PAGE29: DEL R243 in BOM. The footprint is shortpad.

PAGE9: Change Clear CMOS pin to GPIO22, combine with BIOS\_REC

PAGE26: Change L65 footprint from 0805 to choke-lqh32pn4r7nn0l

PAGE19: Change GPU VID[5:0] 101010 to 0.9750V

PAGE19: stuff VR122 & VR123 for pulling up GPIO8 & GPIO9,  
GPIO8, 9 & 12 should not be floating during operation,  
it may cause slowdown(DG-05587-001, chapter 16)

PAGE5: Exchange WEBCAM USB D+ and D- for error correct

PAGE16: Add pull high RES for CRT conn.

PAGE19: 64Mx16 DDR3 Hynix strap 0x2

(ROM\_Si pull down with a resistor of 15K 1%)

128Mx16 DDR3 Samsung strap 0x7

(ROM\_Si pull down with a resistor of 45.3K 1%)

PAGE22: By Pass SMBus signal to MMB

PAGE4: Change +1.5V\_CPU to 1.5V\_S3 for cost down.

;DEL Q44,Q27,R166,C650,C651,C652,C648

PAGE7,22: Add SPI\_WP# control by PCH; Add Q6,Q7

PAGE33: Change voltage source from 3.3V\_S0 to 3V\_S5

PAGE34: (1)Add PC35 & PC37 to prevent short through

(2)Change PR23 value from 0.1% to 1%

(2)Change enable signal and voltage source to increase monitor mode

PAGE35: (1)Change PC76 from 47p to 68p to slow slew rate

(2)Change PC89 from 0.15U to 0.22U for RC match

(3)Change PR28 size from 0603 to 0805 for increase drive current

(4)Change PC42, PC43, PC64, PC65, PC83 & PC84 from 4.7U to 10U

(5)Dismount PC86

(6)Add PC56, PC73 & PC94 for transient

PAGE04: (1)Add C50, C560 & C567 for transient

(2)Dismount R406

PAGE36: (1)Add PC36 to prevent short through

(2)Change PL26 from molding type to coil type

(3)Add PC275 & PC276 for output ripple

PAGE38: (1)Add PC39 to prevent short through

(2)Change PR296 & PR298 to 10K

(3)Add PC160 & PC161 for output ripple

(4)Exchange VSSP\_SENSE and VCCP\_SENSE for wrong net

(5)Dismount PR283, PR299 & PC274 and mount PC258

PAGE39: (1)Dismount PR174

(2)Change PR201 & PR202 to 160K

(3)Dismount PC159

(4)Change PC176, PC178, PC271, PC272, PC273 & PC193 from 4.7U to 10U

PAGE40: (1)Add PQ40, PR221 & PC217 for USB S3

(2)Add PQ46, PQ49, PC228, PC229, PR229 & PR232 for monitor mode

PAGE41: (1)Add PQ52, PQ65, PR235, PR251 & PC233 for USB S3

(2)Add PQ74, PC277 & PR29 for monitor mode

(3)Dismount PQ57, PQ58, PR243, PR244

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